पं० रविशंकर शुक्ल विश्वविद्यालय, रायपुर (छ०ग०)

क्र0 139/विकास/2025 रायपुर, दिनांक 04/03/2025

।। दावा आपत्ति सूचना।।

सर्वसधारण को सूचित किया जाता है कि विश्वविद्यालय के उपयोग हेतु निम्नलिखित सॉफ्टवेयर सांपत्तिक प्रवृत्ति (Properietry Article) की श्रेणी के अंतर्गत क्रय किया जा रहा है :–

1. MATLAB Campus wide License (CWL) Software
2. Cadence VLSI University Research Bundle
3. VLSI Lab Tool Under CoreEL University Program
4. Silvaco Victory 3D Bundle Research Bundle

सांपत्तिक क्रय की श्रेणी के अंतर्गत क्रय के संबंध में किसी निर्माता कंपनी को यदि कोई आपत्ति हो तो दिनांक 04/04/2025 तक मयसुसंगत दस्तावेज विकास विभाग, पं.रविशंकर शुक्ल विश्वविद्यालय, रायपुर (छ.ग.) में प्रस्तुत करें। दिनांक 04/04/2025 के पश्चात प्राप्त दावा आपत्ति पर कोई विचार नहीं किया जायेगा।

4/3/25

कुलसचिव

pm USHA (Electronics)
Purchase

20/2/25

SILVACO
SILVACOSINGAPOREPTELTD

Dated:February 20th ,2025

Sent via email

Pt. Ravishankar Shukla University
Great Eastern Rd. Amanaka Raipur
Chattisgarh-492010

Letter of Authorization and Proprietary Certificate
For
Pt. Ravishankar Shukla University

DearMadam/Sir,

Subject: **Letter of Authorization and Proprietary Certificate for Silvaco tools in India**

This is to confirm that Cognitive Design Technology Pvt. Ltd. (CDT), located at No:93/2- 1, 2nd Floor 12th Cross, Margosa Road, Malleshwaram, Bengaluru – 560 003, India is our authorized distributor of Silvaco software products and services for Government, Defense, Commercial,Space,Atomic Research, anduniversities.

This is also to certify that the Athena, Atlas, and their sub modules, the software by Silvaco is articles of a proprietary nature, and weare the original manufacturer/developer of the said Items. The prices of the tools are approved by us.

These items are solely manufactured/developed by SILVACO and not by any one else in the entire world.

Sincerely,

赵庆达

SILVACO
Silvaco Singapore Pte Ltd

Yours Sincerely,
Zhao Qingda
ManagingDirector
SilvacoSingaporePteLtd

Victory Mesh

Meshing and Solid Modeling

SILVACO

Overview

Victory Mesh provides users with power functionality to mesh and refine exiting 2D and 3D TCAD structures, as well as solid modeling capabilities to generate new 2D and 3D structures.

Executable from within the Deckbuild TCAD graphical user interface, Victory Mesh accepts input such as:

- Silvaco standard structure file format (.str) in 2D and 3D
- Saved status from Victory Process semiconductor process simulator in 2D and 3D

Victory Mesh outputs can be:

- Visualized within TonyPlot (2D) & TonyPlot3D (3D)
- Exported to semiconductor device simulators Victory Device, Atlas, and Clever
- Exported in standard formats (e.g. .stl and .vtk) to 3rd party software

Device Meshing - Victory Mesh provides a selection of schemes for meshing of devices:

- Delaunay (unstructured sampling)
- Conformal (semi-structured Cartesian-based sampling)

Device Refinement (Remeshing) - Victory Mesh includes a number of Delaunay refinement schemes, both general and TCAD-specific:

- Uniform
- Impurity
- Junction
- Interface
- Shape
- Approximation Distance
- Quality

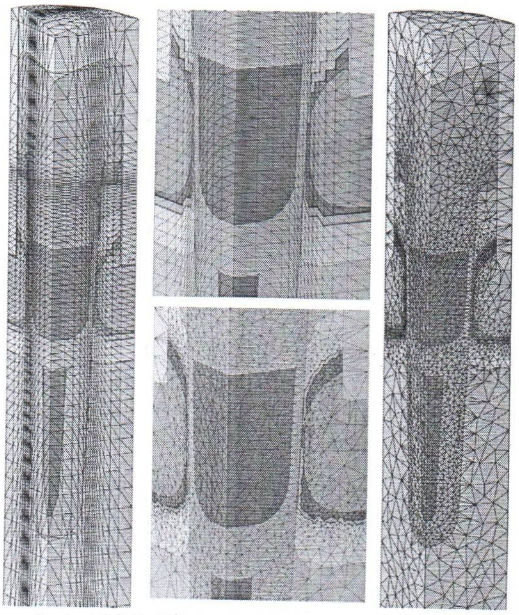
Solid Modeling - Victory Mesh contains a number of features to generate devices directly within the Victory Mesh engine:

- Shape Generation
- Geometric Transformation
- Mirror
- Join
- Crop
- Slice
- Combine
- Splice

Mesh Generation and Remeshing

Victory Mesh takes raw geometrical data from Victory Process as input and produces a mesh that is suitable for device simulations in Victory Device, Atlas, and Clever.

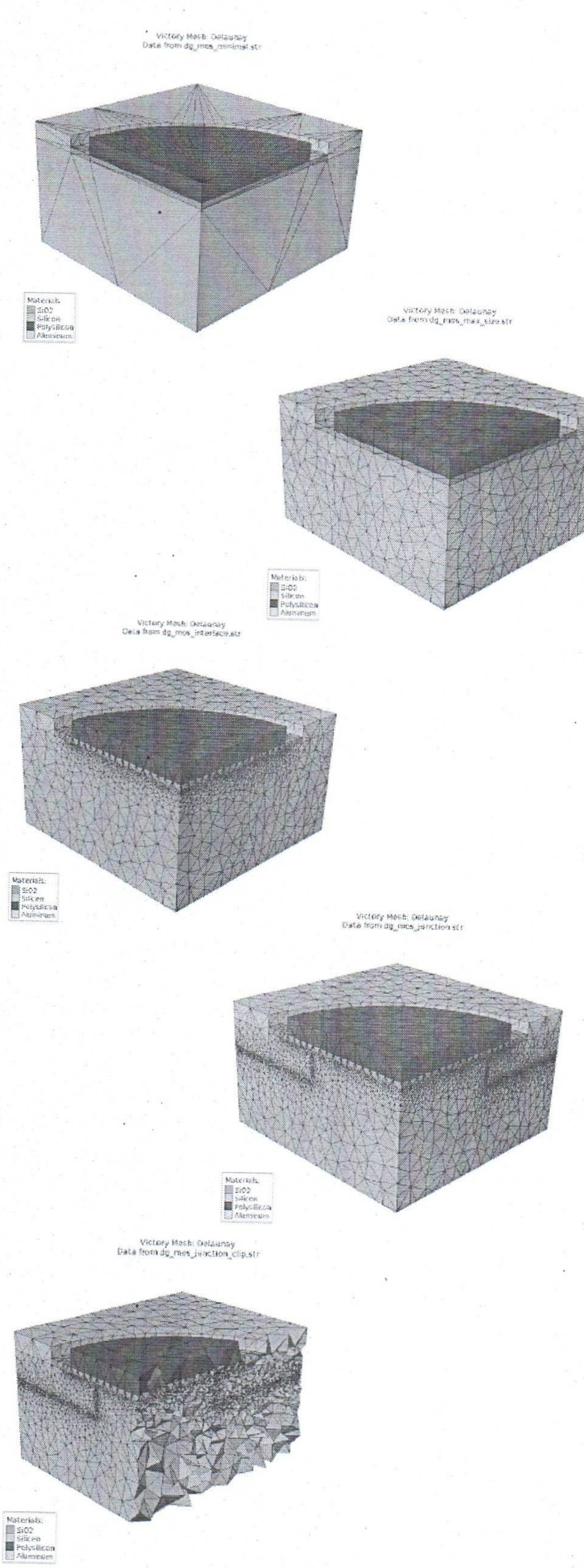
There are two basic types of mesh structure that can be output from Victory Mesh and both of these mesh types can be used in Silvaco device simulators.



Conformal (left) - User specified structured Cartesian mesh.
Delaunay (right) - Automated feature and quantity-dependent unstructured mesh.

Features

- User-defined mesh (Conformal) or automatic parameter defined (Delaunay) in either 2D or 3D
- Delaunay mesh can be automatically generated to prioritize any number of:
  - o Specific volumetric materials
  - o Specific interface material combinations
  - o Specific distances from interfaces
  - o Specific volumetric quantities
  - o Specific physical locations
- Flexibility to choose mesh type and density to suit specific simulation needs



Example structure showing Delaunay meshing with automatic refinements by: max element size, interface refinement, junction refinement. Cut-away slice shows internal mesh refinement within structure.

Solid Modeling

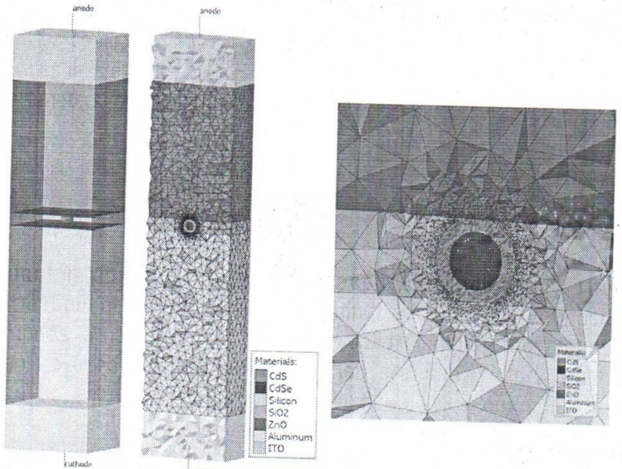
Victory Mesh contains support for generating various types of shapes in 2 and 3-dimensions, such as:

- 2D – Triangle, Rectangle, Circle, etc.
- 3D - Cone, Cuboid, Cylinder, Ellipsoid, Pyramid, Sphere, etc.

Shapes are generated consisting of a user-specified material. These shapes can subsequently be used in other commands such as REFINE, CROP and JOIN. Each type of shape can be generated by an individual command. The syntax is designed to be as consistent as possible between 2- and 3-dimensions. The dimension of the result is usually implied by the dimension of the points used as parameters to define the shape.

Application Example – Quantum Dot

Quantum dots are of interest in recent LED technology. The formation of a quantum dot within traditional etch/deposit engines is not practical. However, solid modeling techniques can be used to greatly simplify their creation. Victory Mesh can be used to quickly and easily generate a quantum dot using a number of solid modeling commands. The structure uses Delaunay meshing to create highly detailed mesh near the quantum dot and its interfaces as well as a much coarser mesh in areas of less importance.

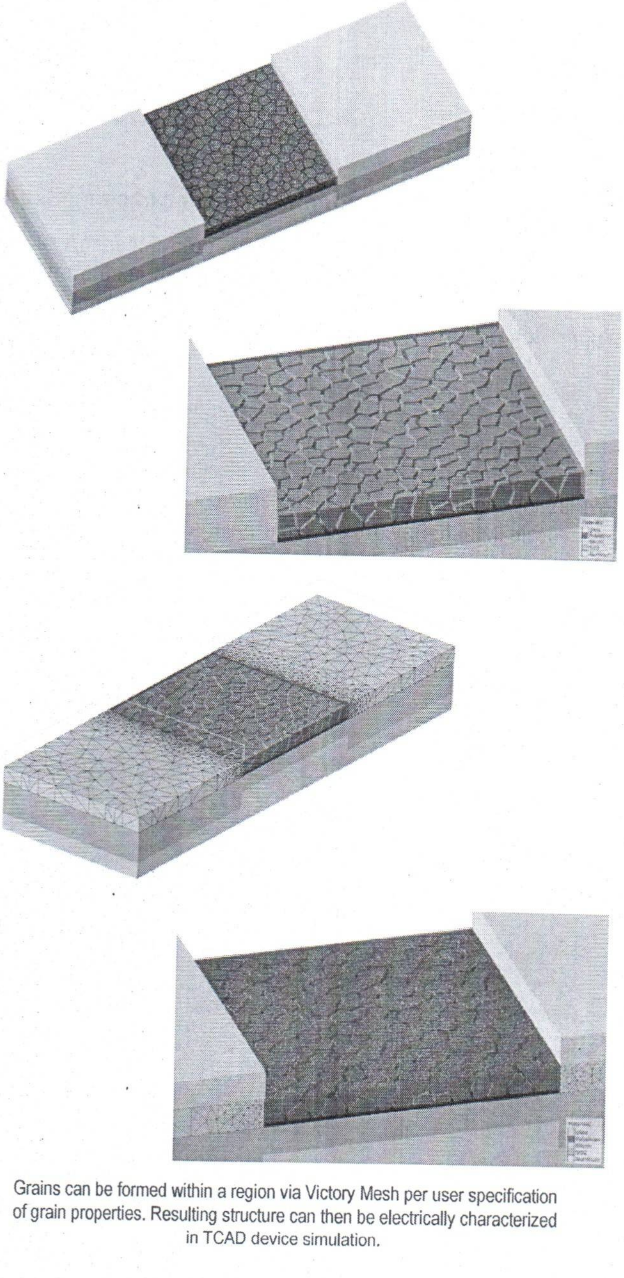


Transparent view of semiconductor regions to make the quantum dot visible. Mesh slice view to internal mesh of the structure. Close view showcasing the fine detail resolution of the mesh.

Application Example – Grain Generation

Laser Annealing processes, such as Excimer Laser Annealing (ELA) are used to convert amorphous silicon to polycrystalline silicon and enhance carrier mobility. The poly-Si structure (grain boundary) is dependent on the laser wavelength, pulse width and spatial beam.

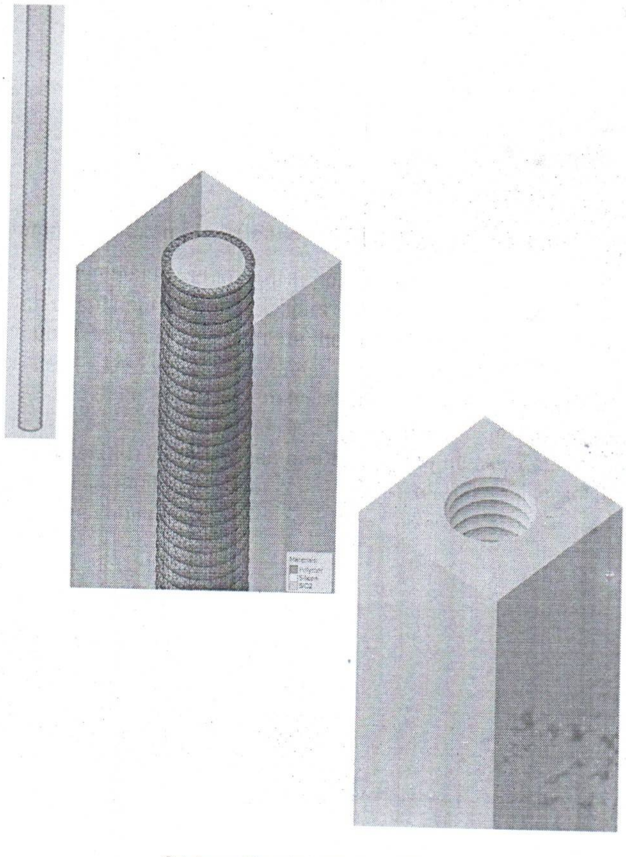
Victory Mesh can emulate grain boundaries formation using a Voronoi discretization. This Grain Generation Example extends beyond the work published in the Simulation Standard article: 3D TFT Simulation of Grains and Grain Boundaries, Vol 29, No. 1 Jan-Mar 2019. Here the grain sizes are varied in all directions.



Grains can be formed within a region via Victory Mesh per user specification of grain properties. Resulting structure can then be electrically characterized in TCAD device simulation.

Application Example – Scalloped Sidewall

Deep Reactive Ion Etching (RIE) process is commonly used to etch deep, nearly vertical, pillars. Silvaco's process simulator (Victory Process) can simulate the Deep Reactive Ion Etching process, however the simulation time associated with this type of detailed process analysis can be time-consuming for very deep trenches. If a user is interested in the device simulation instead, Victory Mesh can be used to quickly generate the geometrical shapes of this process directly using solid modeling commands.



Cutplane of the whole structure (left).
View showing the trench interior (center).
View showing the silicon etch shape without the trench filling (right).

Application Example – Textured Solar Cell

To enhance light absorption, solar cells have been manufactured with textured surfaces. For crystalline silicon, anisotropic etching with enhanced etch rates along preferential low index directions generates complex surface pyramids. This is computationally costly to perform in process simulation. An alternative approach is to use solid modeling. This texture solar cell is generated using the Victory Mesh solid modeling commands. The structure is also remeshed in Victory Mesh using Delaunay remesh scheme to refine on dopants and the oxide interface. The mesh can then be loaded in Silvaco's Device Simulators for device characterization.

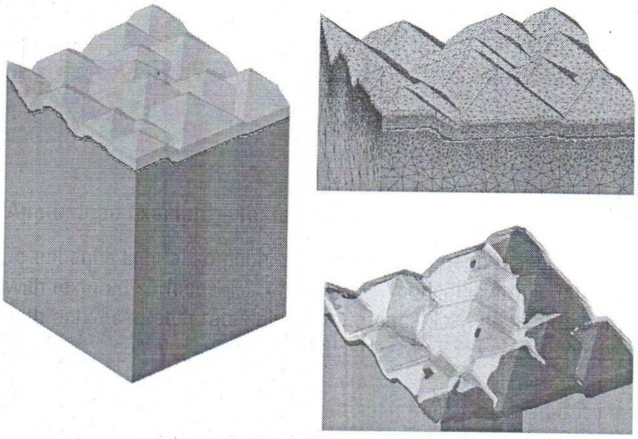
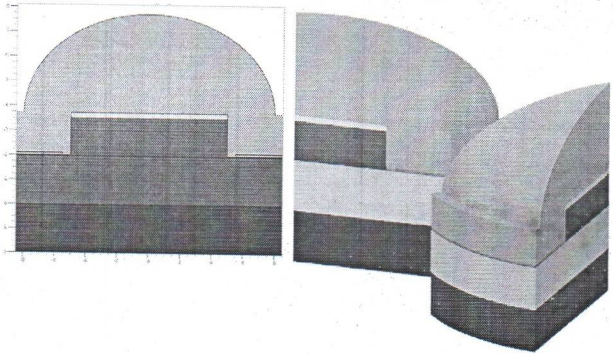


Image of the full structure made in Victory Mesh. Image showing Delaunay refinement on dopant and interfaces. Image of the structure imported into Victory Device and showcasing spreading current density throughout the textured surface.

Application Example – MicroLED

A typical micro LED structure contains many tightly spaced layers of material. These devices are relatively simple to generate within standard etch/deposit process engines. However, the cap stage is more complex. Victory Mesh can generate a micro LED entirely using solid modeling commands. This LED also contains a realistic cap stage. The mesh can then be loaded in Silvaco's Device Simulators for device characterization.



Using the solid modeling engine, a multi-layer GaN LED with capping layer can be generated.

Input Deck

Victory Process Structure Files

Victory Mesh
Inputs/Outputs

User-Specified Structure file (.str, .stl, .smp, .lay)

Run-time Output

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Victory Device

2D/3D Device Simulation

SILVACO

Victory Device provides versatile simulation capabilities for physically based two-dimensional (2D) and three-dimensional (3D) semiconductor devices, performing DC, AC, and transient analysis of silicon, binary, ternary, and quaternary material-based devices.

Victory Device is a physics-based platform that is modular, easy to use, and scalable. A tetrahedral meshing engine is used for fast and accurate simulation of complex 3D geometries. Efficient and robust multi-threaded operation significantly reduces simulation time on parallel CPU machines while maintaining high accuracy.

Key Features

- Tetrahedral mesh for accurate 3D geometry representation
- Voronoi discretization for conformal and Delaunay meshes
- Advanced physical models with user-customizable material database for silicon and compound materials
- Stress-dependent mobility and bandgap models
- Highly customizable physical models using the C-Interpreter or dynamically linked libraries
- DC, AC, and transient analysis
- Drift-diffusion and energy balance transport equations
- Self-consistent simulation of self-heating effects including heat generation, heat flow, lattice heating, heat sinks, and temperature-dependent material parameters
- Methods to simulate the electrochemical reaction and transport of an arbitrary number of chemical species
- Advanced multi-threaded numerical solver library
- Atlas-compatible
- C-Interpreter included – C-based user defined model development interface
- Silvaco's strong encryption is available to protect valuable customer and third-party intellectual property

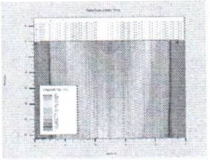
Optical – Photoelectric Devices and Light Absorption Simulation Module

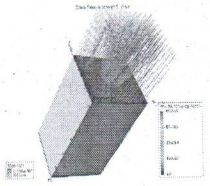
The Optical Module is a 2D and 3D simulation module specializing in light absorption and photoelectric effects modeling of nonplanar semiconductor devices. This module allows you to account for any shape, internal and external reflections and refractions, polarization, and scattering.

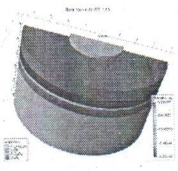
Optical methods include: geometric ray tracing which provides an accurate solution for common light sources; optical transfer matrix analysis of coherence effects in multilayered devices; Beam propagation methods can also be used to simulate coherence effects and diffraction; Finite Difference Time Domain (FDTD) correctly models the wave propagation, including reflection, diffraction, and interference effects.

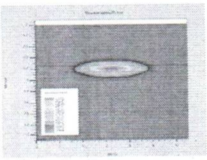
Applications include:

- Solar Cells
- Photo-detectors
- Image Sensors (CMOS, CCD, Visible, LWIR)
- LEDs
- Lasers
- Lenslets



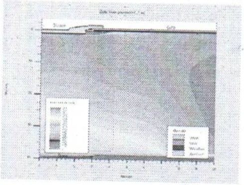






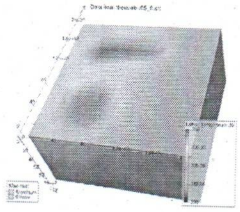
Giga – Device Thermal Analysis Simulation Module

The Giga Module is a 2D and 3D simulation module that analyzes the effects of self-heating into a device simulation. Giga includes models for heat sources, heat sinks, heat capacity and thermal conduction. Physical and model parameters become dependent on the local lattice temperature where appropriate, allowing the self-consistent coupling between the semiconductor device equations and the lattice temperature.



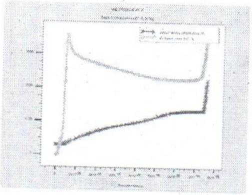
Applications include:

- Heat generation
- Heat flow
- Lattice heating
- Heat sinks
- And temperature-dependent material parameters

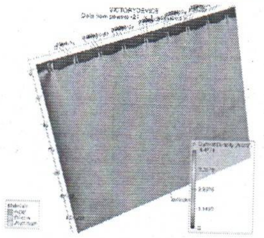


MixedMode - Device and Circuit Mixing Simulation Module

The MixedMode Module is a 2D / 3D circuit simulator that includes physically based devices in addition to compact analytical models. Physically based devices are used when accurate compact models do not exist, or when devices that play a critical role must be simulated with very high accuracy.

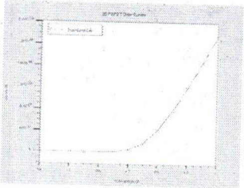


Physically based devices may be simulated using any combination of Victory Device 2D / 3D modules. The physically based devices are placed alongside a circuit description that conforms to the SPICE netlist format. Applications of MixedMode include power circuits, high performance digital circuits, precision analog circuits, high-frequency circuits, thin film transistor circuits, and optoelectronic circuits.



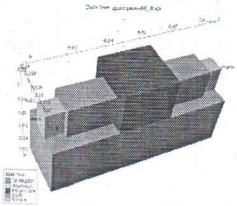
Quantum – Quantum Mechanical Effects Simulation Module

The Quantum Module provides is a 2D and 3D simulation module providing a set of models for simulation of the various effects of quantum confinement and quantum transport of carriers in semiconductor devices. A self-consistent Schrödinger - Poisson solver allows calculation of bound state energies and associated carrier wave function self consistently with electrostatic potential.



Schrödinger solvers can be combined with Non-equilibrium Green's Function (NEGF) Approach in order to model ballistic quantum transport in 3D devices with strong transverse confinement. An alternative approach to modeling subband transport in nanoscale devices is given by Mode-Space Drift-Diffusion Model, which combines transverse Schrödinger with 1D drift-diffusion equations.

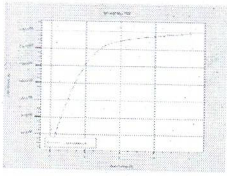
A quantum moment transport model allows simulation of confinement effects on carrier transport and yet keeps the simplicity of a conventional drift diffusion approach. It also allows quantum confinement effects to be included in the energy balance/hydrodynamic transport model. Quantum 3D also models the effects of oxide tunneling.

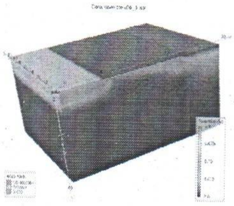


TFT – Amorphous and Polycrystalline Device Simulation Module

The TFT Module is a 2D and 3D simulation module equipped with the physical models and specialized numerical techniques required to simulate amorphous or polysilicon devices in 2D or 3D. TFT models the electrical effects of the distribution of defect states in the band gap of noncrystalline materials.

Users can specify the Density Of States (DOS) as a function of energy for amorphous silicon and polysilicon for grain and grain boundaries as well as the capture cross-sections/lifetimes for electrons and holes. Models for mobility, impact ionization and band-to-band tunneling can be modified to accurately predict device performance.

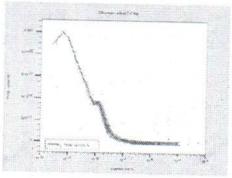


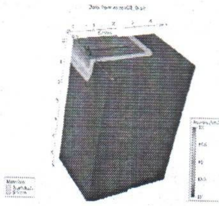


REM / SEE – Radiation Effects and Single Event Effects Simulation Modules

The Radiation Effects Module (REM) and Single Event Effects (SEE) Modlues are 2D and 3D simulation modules which enables modeling of total dose, dose rate, SEU and SEE effects in semiconductors through the generation of defect states, fixed charge, and charge transport within insulating materials.

- Total dose effect on insulators – electron and hole-to-generation, recombination, carrier transport, traps, and de-trap
- Single event effect – charge generation as a function of photocurrent density and linear energy transfer
- Dose rate effect – light generation and recombination, and current flow in the device
- Displacement damage modeling – non-ionizing energy loss model that changes material life, more detailed modeling with user-defined lattice defect modeling layers

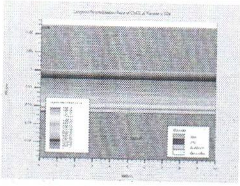




Chemistry – Electrochemical Reaction and Transport Simulation Module

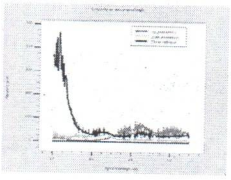
The Chemistry Module enables 2D and 3D modeling of the transport and reaction of chemical species within the body of a semiconductor device. These capabilities may be used for studies of performance degradation, simulation of complex charge-capture mechanisms, and for the simulation of charge-transport by atomic species, as well as for investigating the behavior of novel devices.

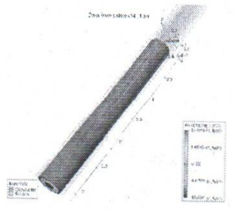
Chemistry is able to simulate the transport and reaction of an arbitrary number of chemical species, limited only by time constraints and the availability of memory in your computer.



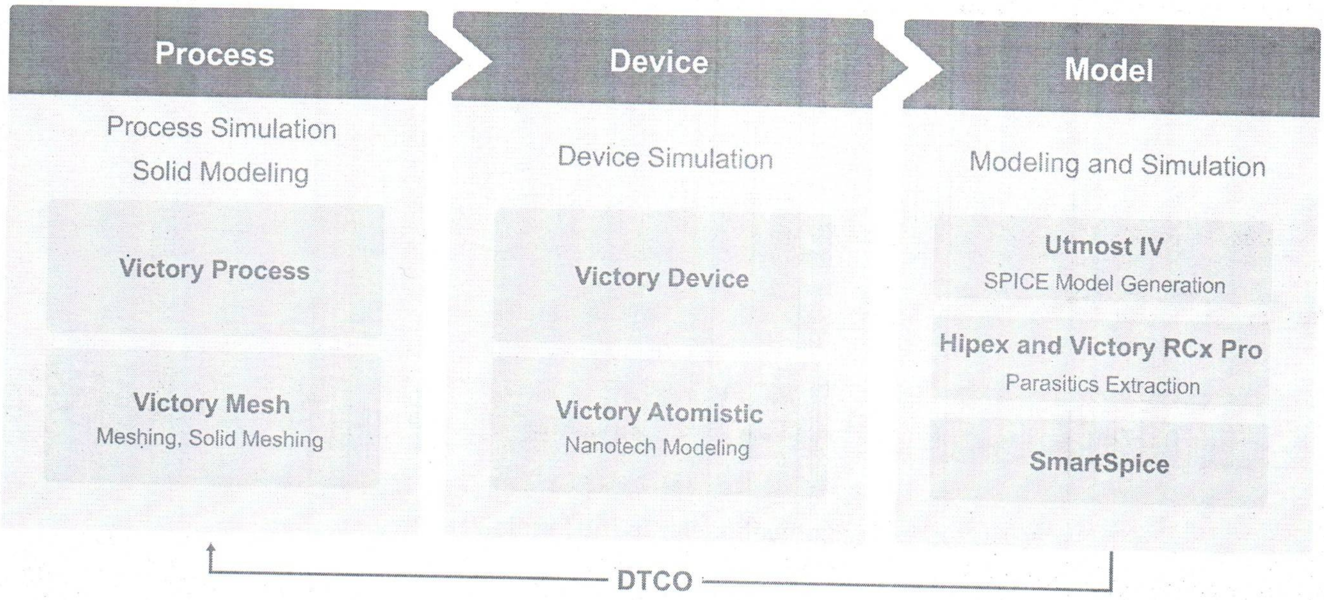
Organic – Organic Semiconductor Devices Simulation Module

The Organic Module enables 2D and 3D simulation of semiconductor devices composed of organic materials. Typical organic-based devices include those used in active displays, such as organic field-effect transistors (OFETs) and organic light-emitting diodes (OLEDs), as well as light-sensitive devices such as solar cells and image sensors.





Victory TCAD Product Solutions



Process

Process Simulation
Solid Modeling

Victory Process

Victory Mesh
Meshing, Solid Meshing

Device

Device Simulation

Victory Device

Victory Atomistic
Nanotech Modeling

Model

Modeling and Simulation

Utmost IV
SPICE Model Generation

Hipex and Victory RCx Pro
Parasitics Extraction

SmartSpice

DTCO

Product Name	Product Code
Victory Device 3D Simulator	11004
Victory Device 2D Simulator	11006
Victory Device 3D SEE	11001
Victory Device 2D SEE	11007
Victory Device 2D MixedMode	11008
Victory Device 3D MixedMode	11009
Victory Device 2D REM	11010
Victory Device 3D REM	11011
Victory Device 2D Optical	11012
Victory Device 3D Optical	11013
Victory Device 2D TFT	11014
Victory Device 3D TFT	11015

Product Name	Product Code
Victory Device 2D Giga	11016
Victory Device 3D Giga	11017
Victory Device 2D Chemistry	11018
Victory Device 3D Chemistry	11019
Victory Device 2D Organic	11020
Victory Device 3D Organic	11021
Victory Device 2D Quantum	11022
Victory Device 3D Quantum	11023
Victory Device 2D LED	11024
Victory Device 3D LED	11025

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Victory Process

SILVACO

3D Process Simulator

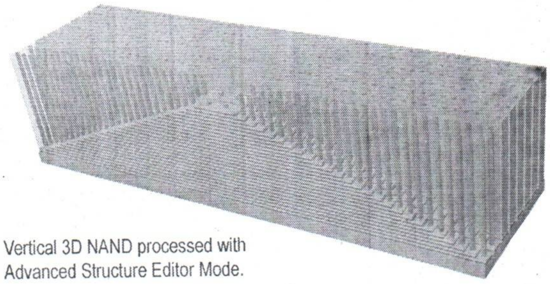
Victory Process is a general purpose layout driven 1D, 2D and 3D process and stress simulator including etching, deposition, implantation, diffusion, oxidation and stress simulation capabilities.

Features

- Fast 3D structure prototyping capability enables the in-depth physical analysis of specific processing issues
- Supports double side wafer processing simulation
- Comprehensive simulation support for compound materials, including variable compositions
- Comprehensive set of diffusion models: Fermi, twodim, single-pair, and five-stream
- Comprehensive full flow stress analysis , including stress induced by lattice mismatch, thermal mismatch, deposition and physical oxidation
- Extremely accurate and fast Monte Carlo implant simulation
- Efficient multi-threading of time critical operations of implantation, diffusion, oxidation, and physical etching and deposition
- Multi-particle flux models for physical deposition and etching with substrate material redeposition
- Open architecture allows easy introduction and modification of customer specific physical models for etching, deposition and annealing
- Seamless link to 3D device simulators including structure mirroring, adaptive doping refinement and electrode specification
- Parametrized layout specification as part of the simulation flow
- Convenient mesh specification based on layout features as well as manual mesh adaptation within the simulation flow
- Easy to learn, powerful debug mode and user friendly SUPREM-like syntax (Athena compatibility)
- Convenient calibration platform and fast process testing with 2D mode (no need to run 3D for calibration)
- Automatic switching from 1D, 2D and 3D mode as well as structure mirroring during process simulation to optimize simulation time

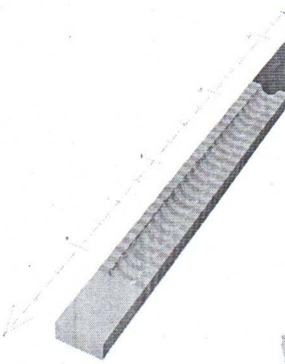
Victory Process has two modes of operation:

- The **Advanced structure editor** mode, also called cell mode, is for fast proto-typing of 3D structures, such as image sensors, SRAM cells or FinFETs, where structure output meshing algorithms are optimized for loading into 3D device simulators for subsequent electrical characterization.

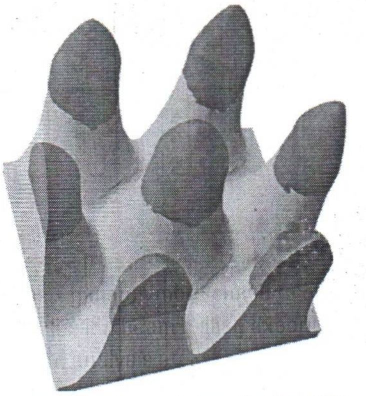


Vertical 3D NAND processed with Advanced Structure Editor Mode.

- **Process simulator mode**, is a full feature, level set based 1D, 2D and 3D process and stress simulator, more suited to process based analysis, such as complex ion beam milling experiments and stress dependent oxidation analysis etc.



Simulation of a gate etch in a 3D NAND with process simulator mode.



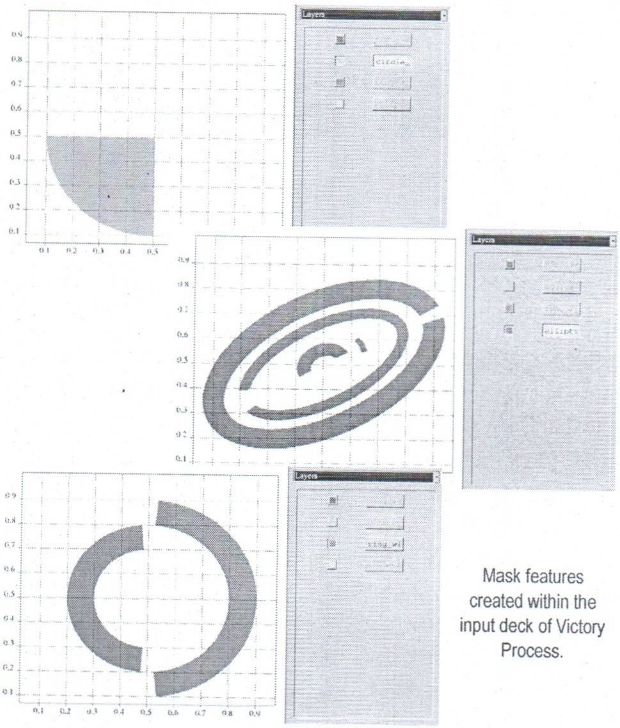
Formation of magnetic tunnel junction pillars simulated in process simulation mode.

This brochure first shows examples and features that are common to both modes of operation, such as implantation, diffusion, epitaxy and stress analysis and then describes features that are exclusive only to the advanced structure editor mode or to the advanced process simulator mode.

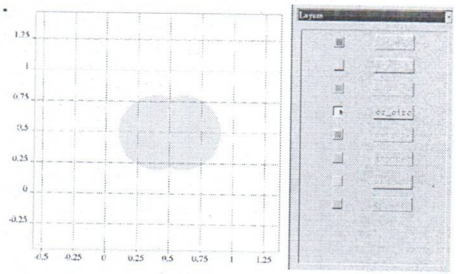
Features Common to Advanced Structure Editor and Process Simulator Modes

Comprehensive Layout Handling

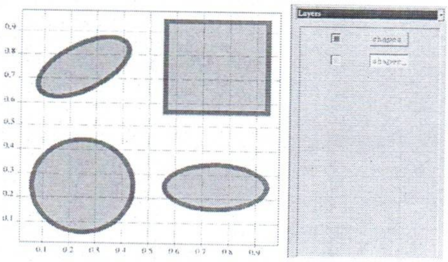
- Specification of layouts within the simulation flow with a comprehensive set of primitives, enables complex parametrized layouts
- Handles predefined layouts in gds as well as SILVACO native mask format
- Allows modification of predefined layouts (shift, resize and boolean operations)
- Generates mask layers on the basis of LVS rule deck



Mask features created within the input deck of Victory Process.



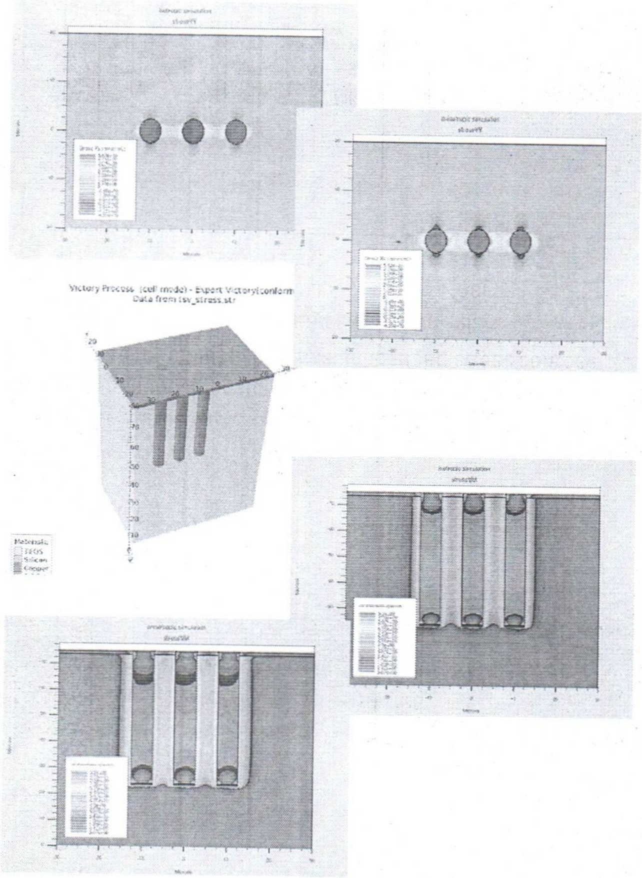
Boolean operations of mask layers by means of the input deck.



Transformation of mask layers by means of the input deck.

Stress History Simulation

- Simulation of the full stress history of all processing steps but also allows for single step stress analysis
- Accounts for multiple processing induced stress sources including deposition induced intrinsic stress, lattice mismatch stress, thermal mismatch stress and oxidation induced stress
- Accounts for stress feedback on oxidation
- Handles graded compound substrates as well as graded epitaxal compound layers



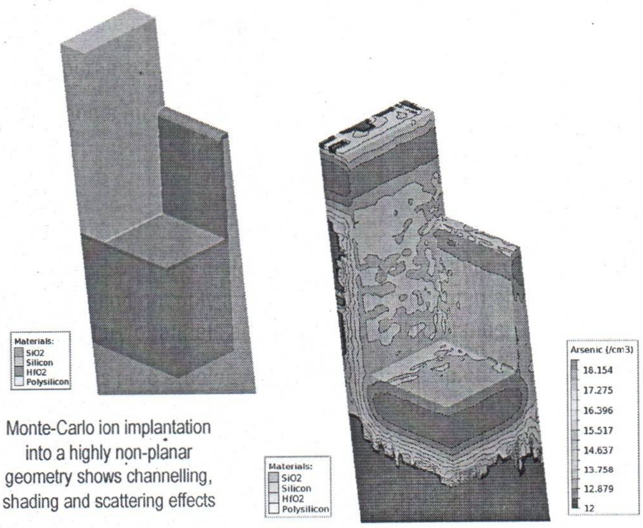
Geometry and stress profile in TSV structure when isotropic (middle) and an-isotropic (right) material properties are applied.

Analytical Ion Implantation

- Experimentally verified Pearson and dual Pearson implant models
- Extended implant moments tables with energy, dose, tilt, and rotation variations
- Support for user specific implantation profiles as well as moment tables
- Fully multi-threaded with run time reduction almost linearly proportional with number of CPUs

Monte Carlo Implantation

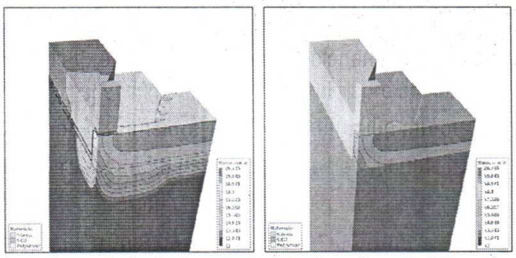
- Supports moments extraction on by Monte-Carlo implantation module
- Supports loading 3D profiles obtained by Monte-Carlo simulation
- Supports loading 1D experimental profiles
- Very accurate ion distributions in both crystalline and amorphous materials forming arbitrary geometries and multi-layer structures
- Supports user defined materials
- Material properties can be configured in the open material database
- Accurately calibrated for wide range of energies starting as low as 200 eV and spanning to the high MeV range
- Calibrated implantation into diamond and hexagonal type crystalline materials : Silicon, SiC, GaN
- Support arbitrary substrate orientation
- Accounts for all complex implantation effects such as reflections, re-implantation and shadowing even in deep trenches and voids
- Handles arbitrary implant directions
- Applies 3D binary collision approximation which predicts channeling not only into primary channel but in all possible secondary channels and crystallographic planes
- Provides time efficient and cost effective solutions for important technology issues such as shallow junction formation, multiple implants and pre-amorphization, HALO implants, retrograde well formation, and well proximity effect
- Fully multi-threaded with run time reduction almost linearly proportional with number of CPUs



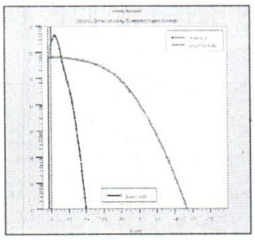
Monte-Carlo ion implantation into a highly non-planar geometry shows channelling, shading and scattering effects

Diffusion

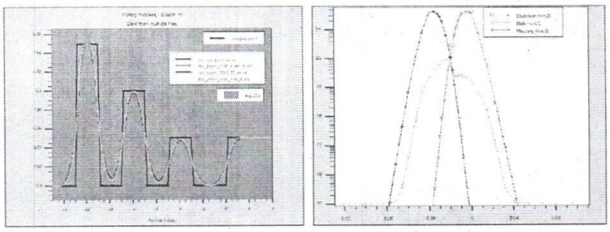
- Twodim, Fermi and grainbased diffusion model compatible with Athena/SSuprem4
- Simulation of multiple dopant diffusion
- Accounts for solid solubility, dopant activation, and segregation at material interfaces
- Continuity interface conditions for materials with sharp change in composition, like Silicon to SiGe or two regions of SiGe
- Fully multi-threaded equation assembler and linear solver provide substantial speed improvement on multi-core computers
- Simulation of transient enhanced diffusion effects
- Three-stream and five-stream diffusion models
- Point defect trapping and clustering models
- Impurity segregation at all material interfaces
- Impurity activation and solid solubility
- Diffusion in compound semiconductors like HgCdTe, InP, SiGe, SiGeC taking into account composition dependencies
- Simulation of the re-distribution of the material composition in compound semiconductors like HgCdTe
- Discontinous material interface model for heterostructure devices
- Simulation of oxidation mediated diffusion
- Simulation of flash annealing as well as laser annealing with user defined temperature profiles which can vary in time and space



Boron distribution in a complex structure after analytical implant and Fermi diffusion.



Comparison of Fermi and 3-stream diffusion model in the presence of interstitial super-saturation.



Re-distribution of the HgCdTe composition due to annealing at various temperatures - Cadmium and Mercury as well as the dopants are diffusing simultaneously.

Diffusion

- Epitaxial growth of single atomic as well as compound material
- Accounts for doping re-distribution during epitaxy
- Handles graded composition during epitaxy
- Support for complex temperature profiles

Open Material Database

- Full access to all material and modeling data
- Supports user specific material databases and well as simulation specific material databases
- Definition of simulation specific materials by interitance
- Functional layer of the material database enables convenient modification as well as extension of material models
- Interface to open annealing model library for advanced material model development
- All Victory Products share one material database

Open Modeling Interface Capabilities

- Definition of model species
- Definition of model parameters
- Definition of reaction functions
- Configuration of the PDE system

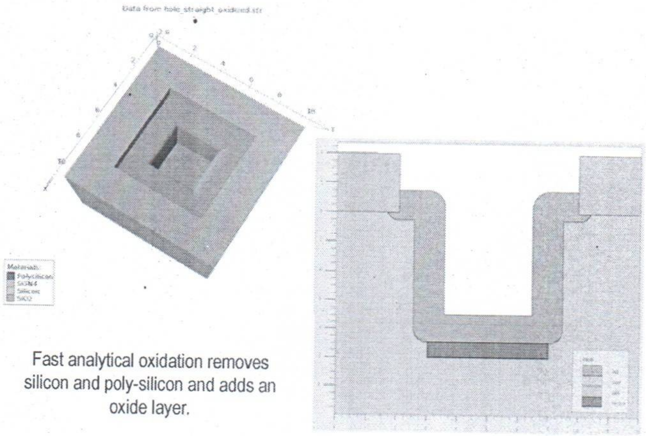
Device Meshing Interface

- Support for various mesh types
- Extensive refinement capabilities for all mesh types including global refinement, interface refinement, junction refinement, shape refinement
- Supports aspect ratio aligned an-isotropic meshing
- Structure modification by mirroring, cropping and slicing operations

Advanced Structure Editor Mode

Fast Geometrical Etching Deposition Empirical Oxidation

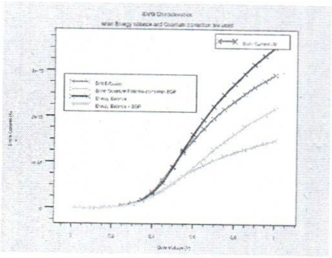
- Unstructured mesh to represent the structure
- Idealized isotropic and dry etching and planarization
- Selective etching or removal of materials regions
- Idealized conformal and direction deposition - Manhatten mode and curved mode
- Mask Layout-based Processing - Just like in a Fab
- Very fast empirical oxidation which approximates the oxide shape
- Deal-Grove and Massoud models are used in empirical mode



Fast analytical oxidation removes silicon and poly-silicon and adds an oxide layer.

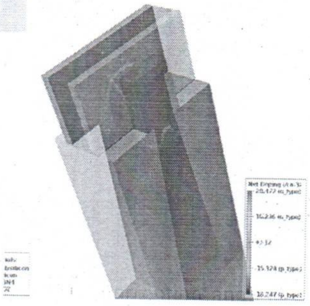
Diffusion

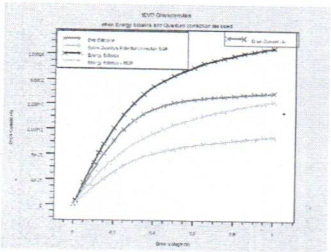
3D FinFET simulated including quantum correction and energy balance.



3D FinFET net doping distribution.

IDVG characteristics, simulated using Victory Device, showing the difference when energy balance and quantum correction are used.

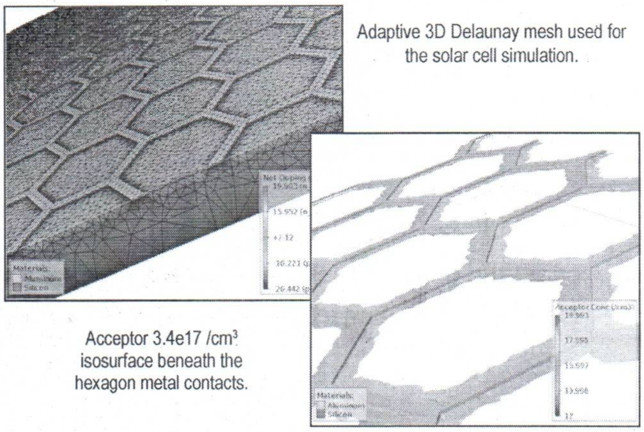




IDVD characteristics, simulated using Victory Device, showing the difference when energy balance and quantum correction are used.

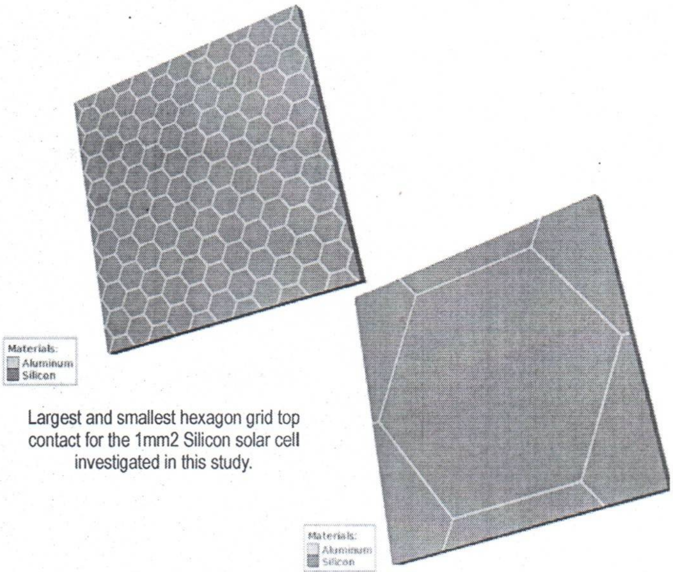
Optical – CIS, CCD, Solar Cells

Among the many design criteria for solar cells, the design of the top metal contact impacts the cell efficiency. The areal density of the top contact modifies the magnitude of the cell output power significantly.

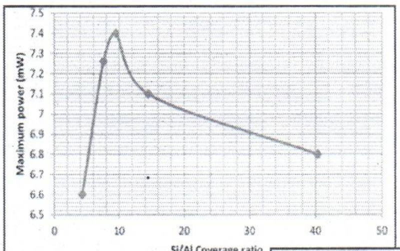


Adaptive 3D Delaunay mesh used for the solar cell simulation.

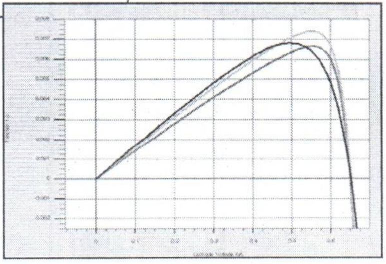
Acceptor 3.4e17 /cm^3 isosurface beneath the hexagon metal contacts.



Largest and smallest hexagon grid top contact for the 1mm2 Silicon solar cell investigated in this study.



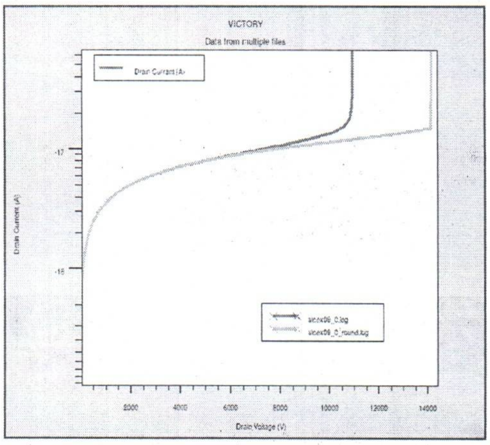
Showing the relationship between the maximum output power and the metal coverage ration R.



Solar cell efficiency with the red trace for the smallest hexagons (circumcircle radius or side length a of 104μm), green (a=225μm) and blue for the largest hexagon (a=945μm).

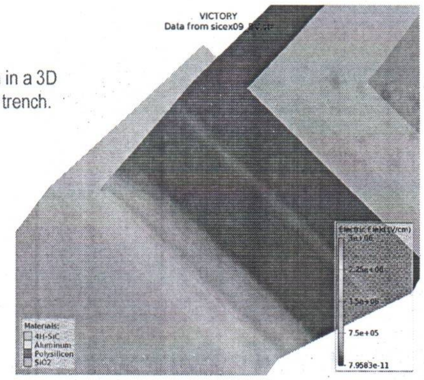
SiC Trench IGBT Example

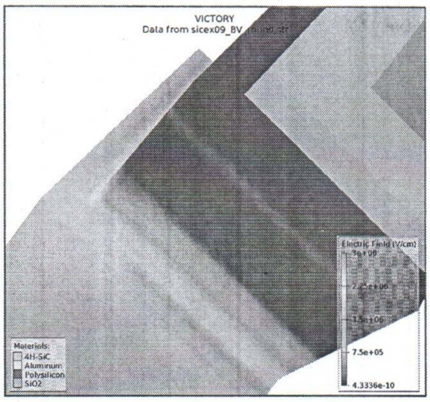
3D trench SiC IGBT simulation shows a ~350V increase in breakdown voltage for a rounded edge trench when compared to a sharp edge trench.



Comparison using Victory Device of 3D IGBT BV simulation results with sharp and rounded trench edges.

Electric field distribution in a 3D IGBT with sharp edge trench.

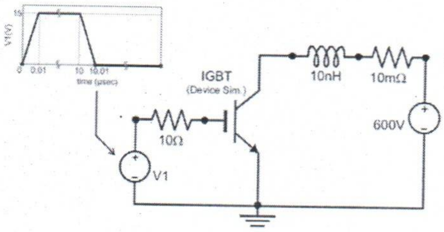




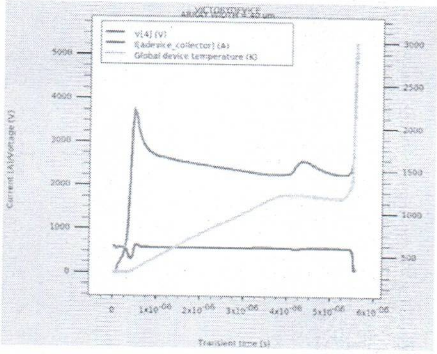
Electric field distribution in a 3D IGBT with rounded edge trench.

3D Current Crowding in Multiple Cells IGBT

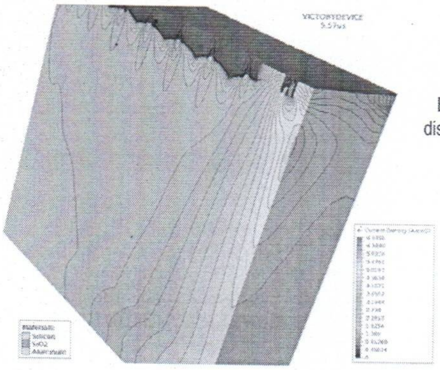
3D TCAD Mixed-Mode simulation of current filaments in IGBT multicell array under short-circuit condition.



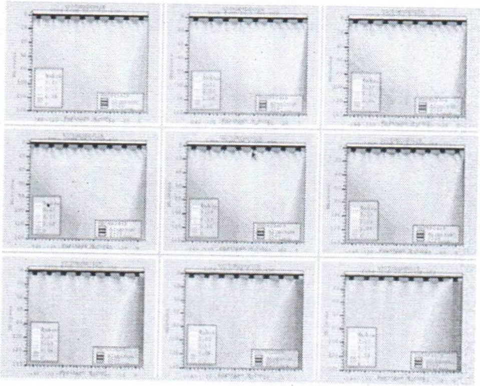
3D Mixed mode short circuit simulation including thermal effect.



Short-circuit waveforms for the 3D 8-cell IGBT array with a width of 40 µm.



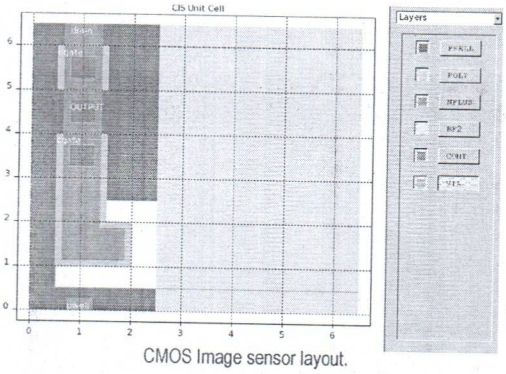
Electron current density distribution at device failure point t = 5.57 µs.



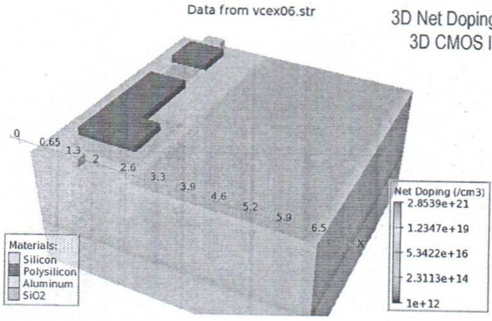
Short-circuit waveforms for the quasi-3D 8-cell IGBT array with a width of 1 µm (b) Cross-sectional views of spatial evolution of electron current density for selected points in time shortly before device burn-out.

CMOS Image Sensor Example

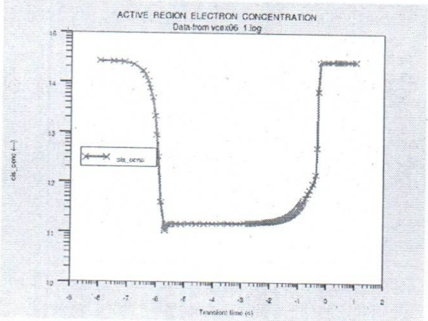
TCAD simulation of the full CMOS image sensor cell, including two pass transistors.



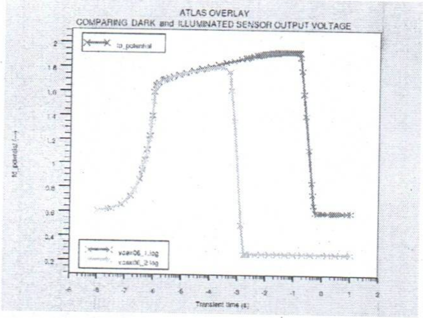
CMOS Image sensor layout.



3D Net Doping distribution in a 3D CMOS Image Sensor.



Electron concentration calculated using Victory Device during dark recovery time simulation.



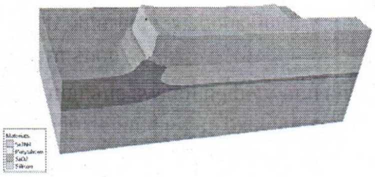
Comparison of sensor output voltage simulation using Victory Device without and under illumination.

Process Simulator Mode

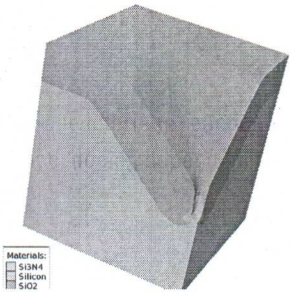
In process mode, the structure is represented implicitly, as a stack of material layers "sandwiched" between surfaces, each surface defined implicitly on the hierarchy of Cartesian meshes.

Oxidation Models

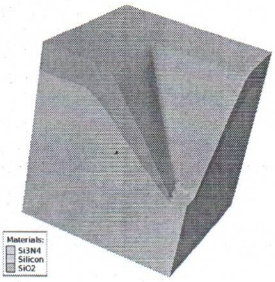
- Oxidation can be simulated in empirical, full physical, or hybrid mode
- Empirical mode is applied for very thin oxidation layers
- Deal-Grove and Massoud models are used in empirical mode
- Full physical mode simulates oxidant transport, reaction on Si/SiO_2 interface, viscous flow, material deformation, and stress formation
- Automatic switching between empirical and full physical mode depending on oxide thickness
- Empirical mode is used in planar regions with coarse mesh allowing layer thicknesses smaller than mesh size to be resolved
- Full physical mode is used in regions with fine mesh
- Stress dependent oxygen transport and interface reaction
- Accounts for orientation dependence, doping dependence and ambient conditions
- Fully multi-threaded with run time reduction almost linearly proportional with number of CPUs
- Oxidation of compound semiconductors like SiGe and SiC also in heterostructure devices



Buffered field oxidation.



Without stress: local oxidation of a quarter section of an inverted pyramid shape using the default linear viscous model.



Stress dependent oxidation of an inverted pyramid. Stress occurs in corner regions. Retardation of the oxide growth due to stress becomes more significant closer to the apex due to the convergence of the corners.

Physical Etching and Deposition Module contains a comprehensive set of models covering a wide variety of topology evolution processes used in semiconductor fabrication and in hard coating for media and tribological applications.

Physical Etch

- Selective etching also with high selectivity
- Isotropic, anisotropic, and directional etching
- Crystal orientation dependent anisotropic etching (e.g., silicon in KOH)
- Plasma etching with material redeposition
- Accounts for particle transport effects and particle and reactor properties
- Multi-particle etching models like ion enhanced chemical etching for deep trench etching in memory technology
- Fully multi-threaded particle flux calculations with run time reduction almost linearly proportional with number of CPUs

Physical Deposit

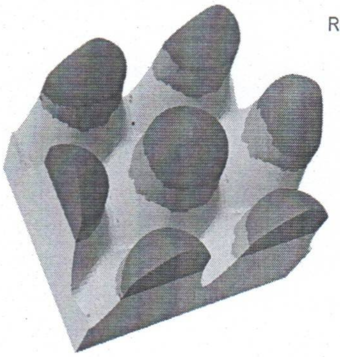
- Conformal, non-conformal, and directional deposition
- Sputter deposition
- Ion assisted sputter deposition
- Accounts for particle transport effects and particle and reactor properties
- Fully multi-threaded particle flux calculations with run time reduction almost linearly proportional with number of CPUs

Open Model Interface Capabilities

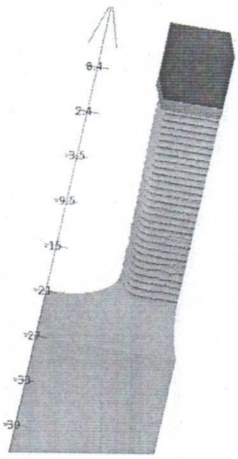
- Very fast empirical approximations for fluxes with multiple reflections
- User definable models for etch rates, conformity, anisotropy, and sticking coefficients
- User specified technological models (e.g., etch rate versus gas flow)
- User definable surface reaction models
- User definable particle transport characteristics through flux models
- All models account for ballistic transport
- Automatic selection of transport mode
- Transport and reaction of multiple particles

Ion Milling (IM) and Ion Beam Deposition (IBD)

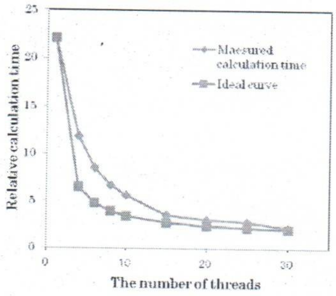
- Static and rotating beams
- Selective switching of rotating beams on and off including redeposition of multiple alloy materials
- Highly collimated and divergent beams for ion beam etching and ion beam deposition
- Capability to simulate re-depositon effects
- Configurable material specific yield functions and re-emission efficiencies
- Accounts for shading effects
- Empirical yield model taking into account processing conditions like ion energy, beam current, ion mass, ion charge

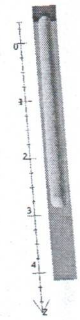


Result of ion milling simulation with redeposition.



Bosch process etch cycle : 7 seconds
deposition cycle : 5 seconds
28 cycles have been simulated





High aspect ration (1:30) trench etching with the ion enhanced chemical etching (IECE) model.

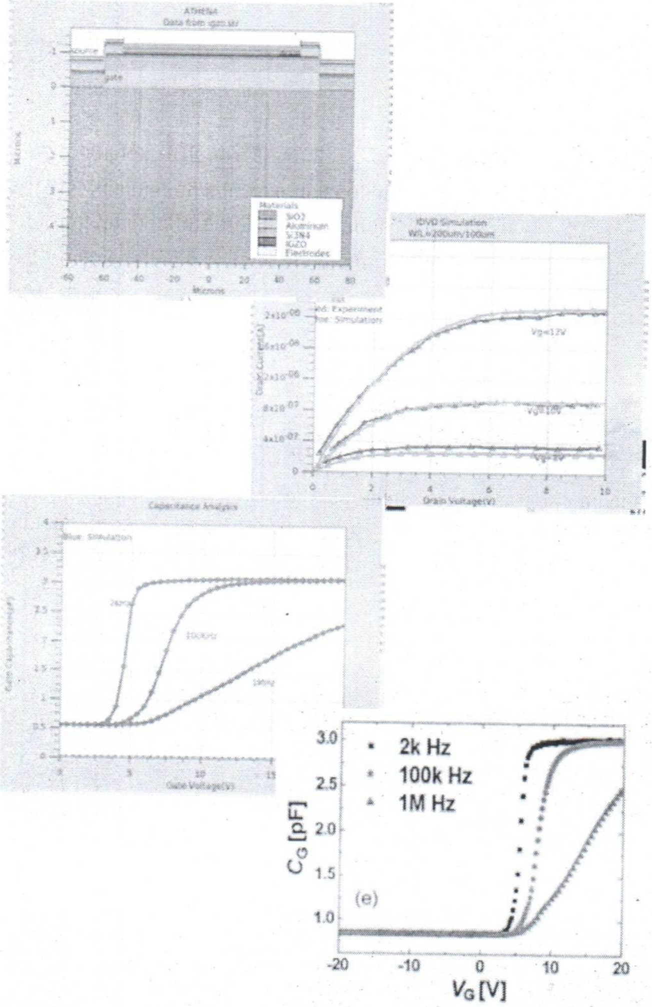
1D and 2D simulation capabilities are available in process mode. Can be considered as a direct replacement for Athena, with mostly compatible syntax for legacy input file conversion.

1D and 2D Mode

- Very similar syntax allows easy migration from Athena and T-Suprem
- Automated input deck conversion within Deckbuild
- Level-set based etch, deposit and oxidation, improves stability for complex structure shapes
- 1D/2D simulation allows quick calibration and process prototyping before full 3D simulation
- Open modeling interface and material database allow custom model development for standard and new materials and dopants
- Seamless link to Atlas and Victory Device
- Multi-threading for most time consuming process steps

a-IGZO TFT Characterization

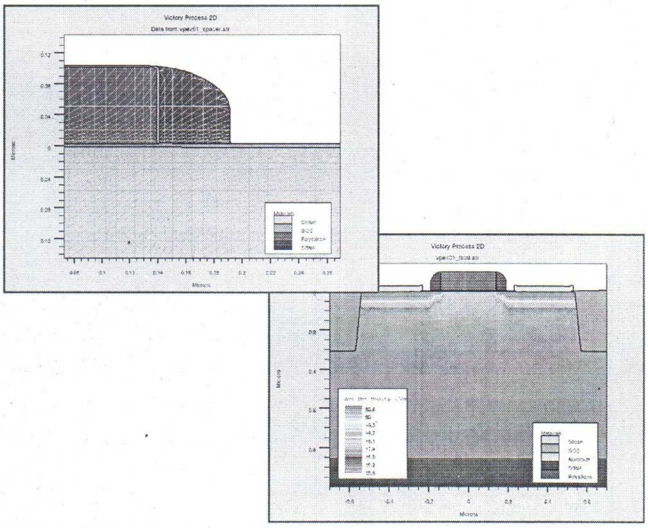
This example demonstrates coupled process and device simulation and characterization of an advanced amorphous InGaZnO thin film transistor used for display applications.



Structure of the a-IGZO TFT obtained by process simulation (left) and IV plot and IdVd plot obtained by device simulation compared to experiments.

28nm MOSFET

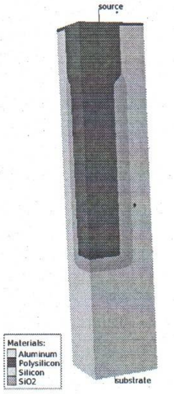
This example demonstrates 2D process simulation for 28nm NMOS transistor with STI (Shallow Trench Isolation). The goal of this example is to demonstrates generic compatibility with Athena.



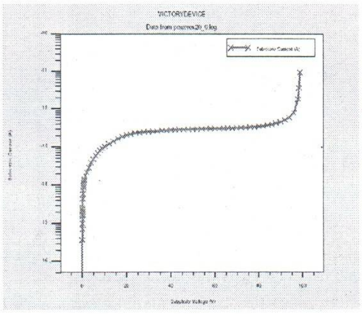
2D process simulation results after 20 process steps including etching, deposition, ion implantation and diffusion/oxidation.

3D Vertical LOCOS Power MOSFET

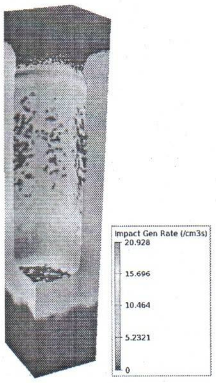
This example shows a 3D curved corner vertical LOCOS MOS power device created by a simplified process flow in Victory Process. The structure is then exported to Victory Device for electrical simulation.



Geometry of the vertical MOSFET.



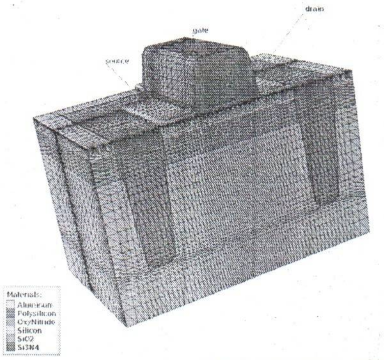
IV curve up to breakdown.

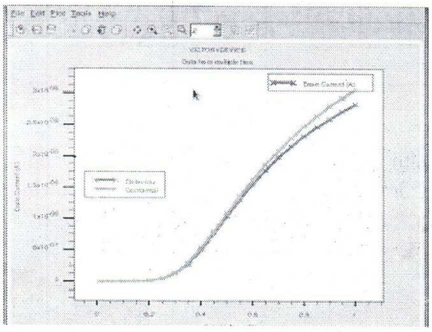


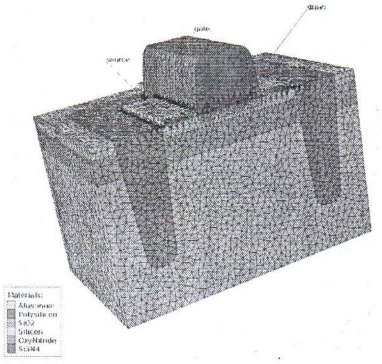
Impact ionization rate near breakdown.

20 nm FDSOI

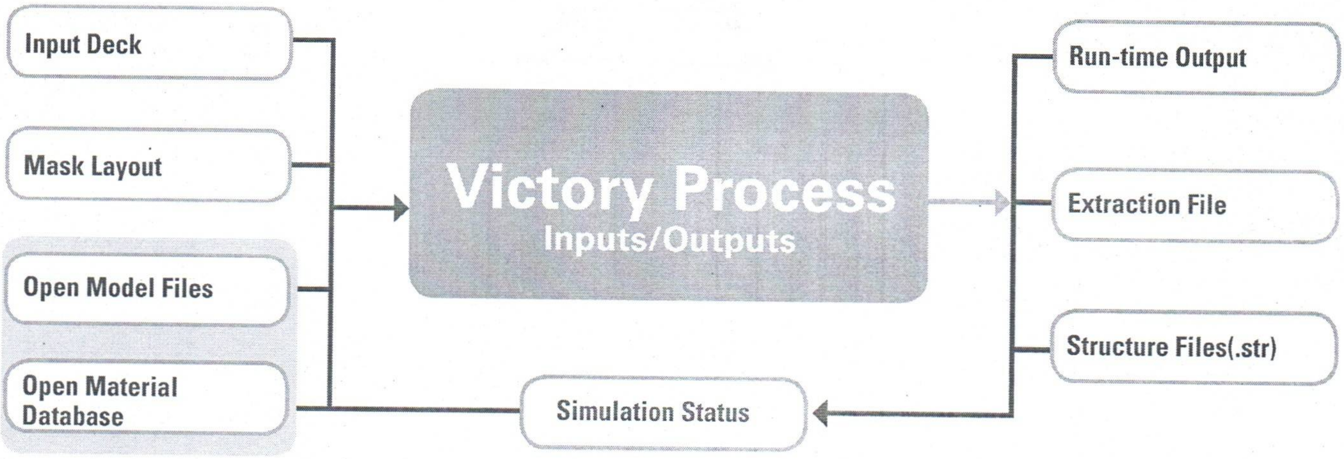
Coupled process and device simulation of narrow 20 nm fully depleted SOI transistor using different device meshing methods.







Analysis of the impact of the mesh shape on the saturation current (top- Victory (conformal) mesh, middle - Victory (delaunay) mesh, bottom - IV curve obtained with different device meshes)



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