पं० रविशंकर शुक्ल विश्वविद्यालय, रायपुर (छ०ग०)

क्र0 139/विकास/2025 रायपुर, दिनांक 04/03/2025

।। दावा आपत्ति सूचना।।

सर्वसधारण को सूचित किया जाता है कि विश्वविद्यालय के उपयोग हेतु निम्नलिखित सॉफ्टवेयर सांपत्तिक प्रवृत्ति (Properietry Article) की श्रेणी के अंतर्गत क्रय किया जा रहा है :–

1. MATLAB Campus wide License (CWL) Software
2. Cadence VLSI University Research Bundle
3. VLSI Lab Tool Under CoreEL University Program
4. Silvaco Victory 3D Bundle Research Bundle

सांपत्तिक क्रय की श्रेणी के अंतर्गत क्रय के संबंध में किसी निर्माता कंपनी को यदि कोई आपत्ति हो तो दिनांक 04/04/2025 तक मयसुसंगत दस्तावेज विकास विभाग, पं.रविशंकर शुक्ल विश्वविद्यालय, रायपुर (छ.ग.) में प्रस्तुत करें। दिनांक 04/04/2025 के पश्चात प्राप्त दावा आपत्ति पर कोई विचार नहीं किया जायेगा।

कुलसचिव

Xilinx, Inc.
Xilinx Ireland Unlimited Company
Xilinx Sales International Pte. Ltd.
2100 Logic Drive
San Jose, CA 95124

AUTHORIZATION CUM PROPRIETARY LETTER

To Whom It May Concern

This is to confirm that CoreEL Technologies (India) Private Limited ("CoreEL") is the preferred Authorized Reseller[1] of Xilinx Products[2] to academic institutions in India effective 20 September 2024 to 19 September 2025.

This is to confirm that CoreEL is the preferred Authorized Training Provider[3] of training courses for Xilinx Products[2] to academic institutions in India effective 12 July 2024 to 12 July 2025.

All Xilinx Products, services, and materials are proprietary to Xilinx. For further information related to the Xilinx product lines and services, we invite you to visit our website: http://www.amd.com.

Sincerely,

Ralph Wittig

Ralph Wittig
Corp. Vice President
Advanced Micro Devices, Inc.

AMD Legal: JTR

1. Subject to the terms and conditions of that certain Reseller Agreement between Xilinx and CoreEL dated 20 September 2024.

2. For the purposes of this letter, the term "Xilinx Products" means products exclusively sold to Xilinx's authorized distributor by only the following subsidiaries of Advanced Micro Devices, Inc. ("AMD"): Xilinx, Inc., Xilinx Ireland Unlimited Company, and Xilinx Sales International Pte. Ltd. (as used herein, individually and collectively, "Xilinx"). The authorization in this letter does not extend to any products exclusively sold directly or indirectly by AMD, or any other affiliate or subsidiary of AMD other than Xilinx, or any of their authorized distributors.

3. Subject to the terms and conditions of that certain Authorized Training Provider Agreement between the parties dated as of 13 July 2023.

SIEMENS

Siemens Industry Software Limited
East Park, Shannon Free Zone,
Shannon, Co. Clare, V14 YD96, Ireland
Tel: +353 (0) 61 256200
Fax: +353 61 256202

January 6, 2025

Sub:- Siemens Industry Software Limited ("SISW") Authorization Certificate

To Whom It May Concern:

SISW produces software products which are best described as Electronic Design Automation software tools, including Computer-aided engineering (CAE) computer tools for design automation industry.

The below listed bundles and corresponding products are proprietary of SISW.

Bundle Name	Products
IC Nanometer Design	Tanner S-Edit, L-Edit, T-Spice, Eldo ®, Questa ® ADMS, Nitro-SoC™, Calibre®
Design Verification Test	Catapult ® University Edition, Vista™, ReqTracer™, Questa (including ModelSim®), Oasys-RTL, Precision ® Synthesis, Leonardo Spectrum™ ASIC, Tessent ® Silicon Test, SystemVision®
Electrical & Wire Harness Design	Capital® Design, Views, Analysis and Harness; Vesys®
PCB with HyperLynx	PADS ® Professional, HyperLynx®
Xpedition with HyperLynx	Xpedition ® with HyperLynx
ODT	ODT (All Technologies)

This letter confirms that CoreEL Technologies (I) Pvt. Ltd. has entered into an agreement with Siemens Industry Software Limited ("SISW") to be an authorized distributor of certain Siemens EDA products, training, and support services in India to SISW customers in India.

CoreEL Technologies (I) Pvt. Ltd. is an independent contractor and is authorized by SISW to license Siemens EDA products subject to terms and conditions at least as protective as the applicable terms and conditions set forth in the distributorship agreement between CoreEL Technologies (I) Pvt. Ltd. and SISW, which may include but are not limited to SISW's standard End User License Agreement together with the EDA Software Supplemental Terms.

This letter is effective until July 6, 2025.

Very truly yours,

S Stringer

Electronically signed by:
Susan Stringer
Date: Jan 7, 2025 08:24 GMT

Director

DESIGN VERIFICATION & TEST

HEP's Design, Verification and Test bundle provides complete solutions for HDL design, verification, synthesis and test of ASICs and FPGAs:

- High level Design and Verification – A comprehensive suite of tools for design creation and analysis using C and System C, including **Catapult C** (University edition) and **Vista**.
- **Questa** Advanced Functional Verification Platform – Completely standards based, **Questa** is the most advanced functional verification product in the industry, supporting assertion based verification, coverage driven verification, test bench automation and formal analysis of clock domain crossing, supported by a comprehensive suite of Verification IP.
- Physical RTL synthesis for advanced-node designs with **Oasys-RTL**.
- FPGA Design and Verification – A complete solution comprising HDL design, simulation, hardware/software co-verification and leading FPGA logic and physical synthesis.
- **Tessent** Silicon Test – A complete technology-leading solution for testability analysis, scan, boundary scan and memory test synthesis, and automatic test pattern generation.
- System Modeling – A complete environment for creation and verification of mixed-signal and Multilanguage systems, prevalent in automotive electrical systems, control systems and mechatronic systems.

DESIGN VERIFICATION & TEST TOOLS

Design Entry & Synthesis		Platform
252991	HDL Designer Ap SW	
232656	Visual SLD Pro Stn SW-MD	
239154	Visual SLD Pro LNL Plus Stn SW	
242631	Visual IP-XACT Ap SW	
264877	Oasys-RTL DFT AddOn SW	
264874	Oasys-RTL Designer Ap SW	
264875	Oasys-RTL Floorplanning AddOn SW	LINUX
264876	Oasys-RTL Low Power AddOn SW	WIN
233858	Precision RTL Plus Ap SW	
211639	Precision RTL Synthesis Ap SW	
204434	Leo Spectrum Lev 3-ASIC Op SW	
204435	Leonardo Insight Op SW	
204436	Spectrum Lev 3 ASIC-VLOG Ap SW	
204437	Spectrum Lev 3 ASIC-VHDL Ap SW	
204439	XLIB Creator Ap SW	WIN

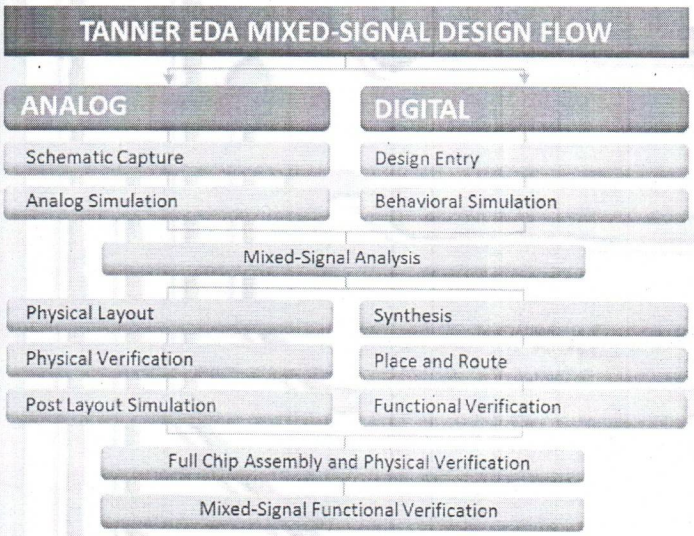
High Level Design		Platform
266210	Catapult C Lib Builder AP	
266339	Catapult-HEP-University Edition Ap SW	
266018	SystemC Input Op SW	LINUX
236144	Vista Architect Stn SW	WIN
235983	ReqTracer Ap SW	

Functional Verification		Platform
248496	Questa Prime Ap SW	
248475	Questa Ultra Bnd SW	
235831	Questa Verification IP Library Ap SW	
248498	Questa Power Aware Simulation Op SW	
248497	Questa Verification Management Op SW	
243168	Questa CDC Ap SW	
252328	Questa Formal Multi-Core Op SW	
258833	Questa Formal AutoCheck Ap SW	LINUX
258834	Questa Formal CoverCheck Op SW	WIN
258835	Questa Formal PropCheck Op SW	
258836	Questa Formal PropGen Op SW	
258837	Questa Formal X-Check Op SW	
222972	Questa CDC-FX Op SW	
258838	Questa CDC ResetCheck Op SW	
271680	Xpedition AMS System Ap SW	
273199	FormalPro Enterprise LEC Ap SW	LINUX
54769	Schematic Generator V8 Ap SW	

Silicon Test		Platform
43879	Tessent FastScan Ap SW	
202287	Tessent FastScan MacroTest Op SW	
211099	Tessent TestKompress Ap SW	
225549	Tessent Diagnosis Ap SW	
260107	Tessent ScanPro Ap SW	
253473	Tessent IJTAG Ap SW	
264637	Tessent MemoryBIST-TS Ap SW	LINUX
264639	Tessent MemoryBIST-TS repair Op SW	
264638	Tessent MemoryBIST-TS field prog Op SW	
273336	Tessent MemoryBIST-TS Automotive Op SW	
265086	Tessent BoundaryScan-TS AC Op SW	
271658	Tessent LogicBIST-NS Ap SW	
268685	Tessent DefectSim Ap SW	
271455	Tessent MissionMode Ap SW	

IC NANOMETER DESIGN

The IC Nanometer Design bundle provides a complete environment for the design, capture, layout and verification of analog, digital and mixed-signal integrated circuits. This bundle includes all products that incorporate the IC Nanometer Design platform:



The **Tanner AMS IC** design flow is a complete end-to-end design flow for analog/mixed-signal (AMS) IC designs. The flow consists of highly integrated front and back-end tools, from schematic capture, mixed-signal simulation and waveform probing to physical layout and foundry-compatible physical verification.

The **Tanner MEMS** design flow delivers 3D MEMS design and fabrication support in one unified environment, and makes it easy to integrate MEMS devices with analog/mixed-signal processing circuitry on the same IC.

The **Questa ADMS** analog and mixed signal verification suite is a language-neutral, mixed-signal simulator that enables top-down design and bottom-up verification of multi-million gate analog/mixed-signal SoC designs. **Eldo and Eldo RF** provides an analog simulator offering numerous simulation and modeling options that deliver high-performance and high-speed simulation with the accuracy required by the user.

The **Nitro-SoC™** and **Oasys-RTL** next-generation synthesis and place and route system comprehensively addresses the time-to-market, performance, capacity, power, area, and variability challenges encountered at the leading-edge process nodes. This advanced physical design implementation tool delivers best-in-class area, power, and performance while significantly reducing design cycle time with a very high design throughput.

The **Calibre** product line is the industry standard platform for physical verification, offering superior performance and capacity for both flat and hierarchical algorithms.

IC NANOMETER DESIGN TOOLS

Custom IC Design (Tanner)		Platform
268927	Tanner Designer Op SW	
266008	Tanner T-Spice AMS Bnd SW	
263719	Tanner SDL Router Op SW	
263700	Tanner T-Spice Bnd SW	WIN
263709	Tanner L-Edit IC Bnd SW	
263711	Tanner L-Edit MEMS Plus Bnd SW	
271113	Tanner Nitro AMS Op SW	
275790	L-Edit Photonics Ap SW	

Analog-Mixed Signal		
250218	Questa ADMS Core MixedHDL Bnd SW	
130007	Artist Link Ap SW	LINUX
212235	Questa ADMS RF Op SW	SUN
204979	Eldo RF Op SW	

Digital Place & Route		
266173	Nitro-SoC P&R Ap SW	
264874	Oasys-RTL Designer Ap SW	
264875	Oasys-RTL Floorplanning AddOn SW	LINUX
264876	Oasys-RTL Low Power AddOn SW	
264877	Oasys-RTL DFT AddOn SW	

IE3D		
250838	HL 3D EM_Acceleration Bnd SW	LINUX WIN

Calibre Design Tools		
61401	Calibre nmLVS-H Op SW	
61498	Calibre nmDRC Ap SW	
61499	Calibre nmDRC-H Op SW	
61501	Calibre nmLVS Ap SW	
67851	xCalibrate Ap SW	
205003	Calibre MT-2nd CPU Op SW	
208309	Calibre CB Ap SW	
210230	Calibre Interactive Ap SW	
210570	Calibre RVE/QDB-H Ap SW	
210681	Calibre DESIGNrev Ap SW	
218002	Calibre xRC CB Ap SW	
221191	Calibre xL Op SW	LINUX
223155	Time-it Op SW	
223993	Calibre ADP Op SW	
225431	Calibre xRC to ADMS Op SW	
226492	Calibre LFD Ap SW	
231096	Calibre YieldServer Ap SW	
234967	Calibre YieldAnalyzer Bnd SW	
234968	Calibre YieldEnhancer Bnd SW	
235811	Calibre PERC Ap SW	
240479	Calibre Auto-Waiver Op SW	
241456	Calibre Pattern Match Op SW	
241971	Calibre InRoute Op SW	

Calibre Design Tools		Platform
242872	Calibre xACT 3D Ap SW	
248337	Calibre RealTime Custom Ap SW	
248461	Calibre xACT SOC Ap SW	
250155	Calibre Multi-Patterning Op SW	LINUX
261024	Calibre xRC Ap SW	
261025	Calibre xACT Ap SW	
271747	Calibre RealTime Digital Ap SW	

Calibre Manufacturing Tools		
203329	Calibre ORC Op SW	
204413	Calibre OPCpro Op SW	
204414	Calibre PRINTimage Op SW	
204415	Calibre PSMgate Op SW	
204416	Calibre WORKbench Ap SW	
205564	Calibre MT-OPCpro Op SW	
207041	Calibre LITHOview Ap SW	
209427	Calibre FRACTUREm Op SW	
210899	Calibre MDPview Ap SW	
211030	Calibre FRACTUREj Op SW	
211565	Calibre nmBias Op SW	
211566	Calibre OPCsbar Op SW	
212329	Calibre FRACTUREt Op SW	
220546	Calibre FRACTUREh Op SW	
220547	Calibre MDPmerge Op SW	
224371	Calibre MPCPro Op SW	
224372	Calibre MDP Embedded SVRF Op SW	
225747	Calibre OPCverify Op SW	LINUX
225771	Calibre ILO Op SW	
226095	Calibre FRACTUREc Op SW	
231209	Calibre FRACTUREv Op SW	
231210	Calibre MetrologyAPI Op SW-LSL3	
231422	Calibre nmOPC Op SW	
235012	Calibre MASKOPT Op SW	
237747	Calibre nmMPC Op SW	
238686	Calibre FRACTUREallSB Op SW	
240233	Calibre MP Manufacturing Op SW	
242811	Calibre nmOPC DDL Op SW	
242817	Calibre Pixbar Op SW	
242837	Calibre nmSRAF Op SW	
248195	Calibre EUV Op SW	
250064	Calibre pxOPC Ap SW	
262694	Calibre MDPDefectAvoidance Op SW	
263057	Calibre WORKbench nmModelflow Op SW	
263147	Calibre OPCverify Classify Plus Op SW	

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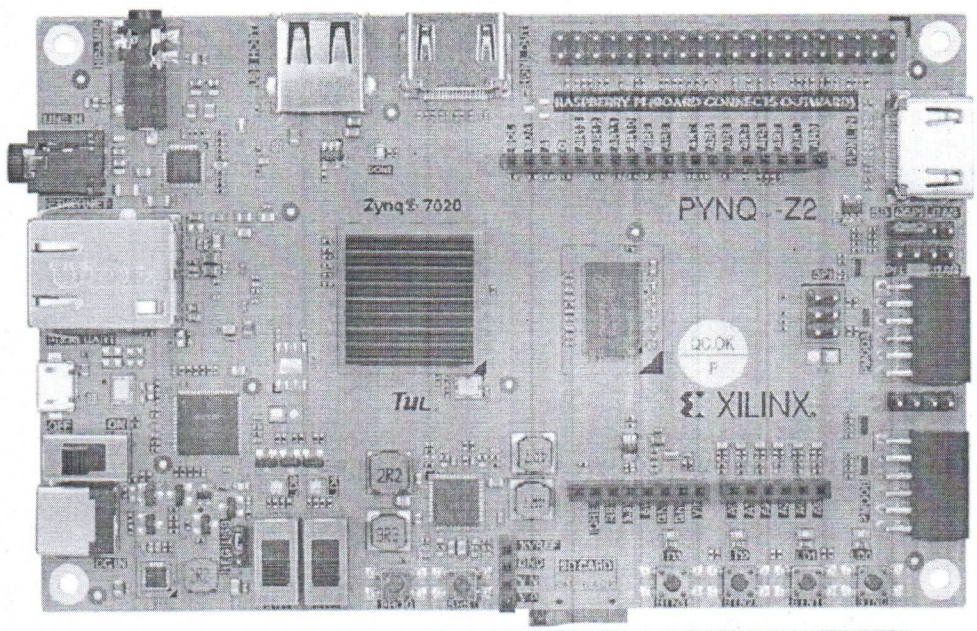
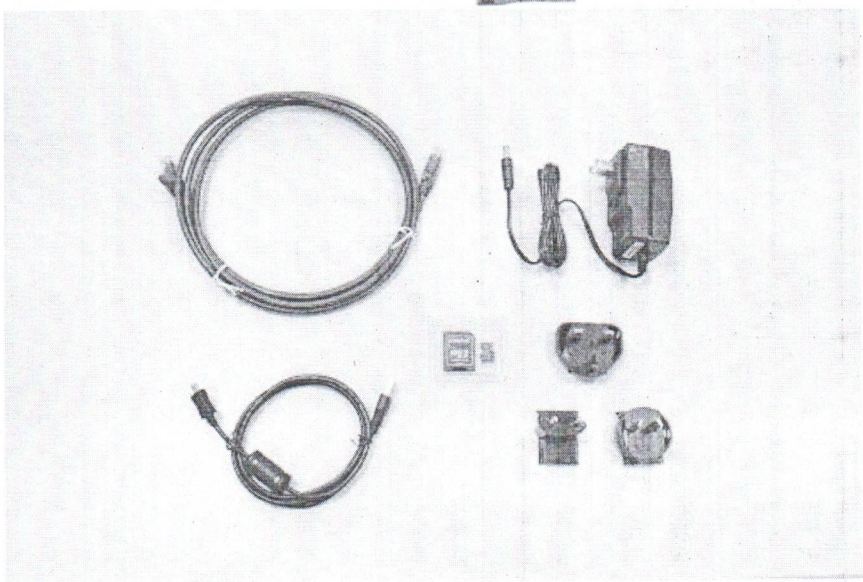
PYNQ-Z2

Part Number: 1M1-M000127DVB





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PYNQ is an open-source project from Xilinx® that makes it easier to use Xilinx platforms.

Using the Python language and libraries, designers can exploit the benefits of programmable logic and microprocessors to build more capable and exciting electronic systems.

PYNQ can create high performance applications with:

- parallel hardware execution
- high frame-rate video processing
- hardware accelerated algorithms
- real-time signal processing
- high bandwidth IO
- low latency control

PYNQ-Z2 features

➢ **ZYNQ XC7Z020-1CLG400C**

- 650MHz ARM® Cortex®-A9 dual-core processor
- Programmable logic
- 13,300 logic slices, each with four 6-input LUTs and 8 flip-flops
- 630 KB block RAM
- 220 DSP slices
- On-chip Xilinx analog-to-digital converter (XADC)
- Programmable from JTAG, Quad-SPI flash, and MicroSD card

➢ **Memory and storage**

- 512MB DDR3 with 16-bit bus @ 1050Mbps
- 16MB Quad-SPI Flash with factory programmed 48-bit globally unique EUI-48/64™ compatible identifier
- MicroSD slot

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- **Power**
  - USB or 7V-15V external power regulator

- **USB and Ethernet**
  - Gigabit Ethernet PHY
  - Micro USB-JTAG Programming circuitry
  - Micro USB-UART bridge
  - USB 2.0 OTG PHY (supports host only)

- **Audio and Video**
  - 2x HDMI ports (input and output)
  - 24bit I2S DAC with 3.5mm TRRS jack
  - Line-in with 3.5mm jack

- **Switches, Push-buttons and LEDs**
  - 4 push-buttons
  - 2 slide switches
  - 4 LEDs
  - 2 RGB LEDs

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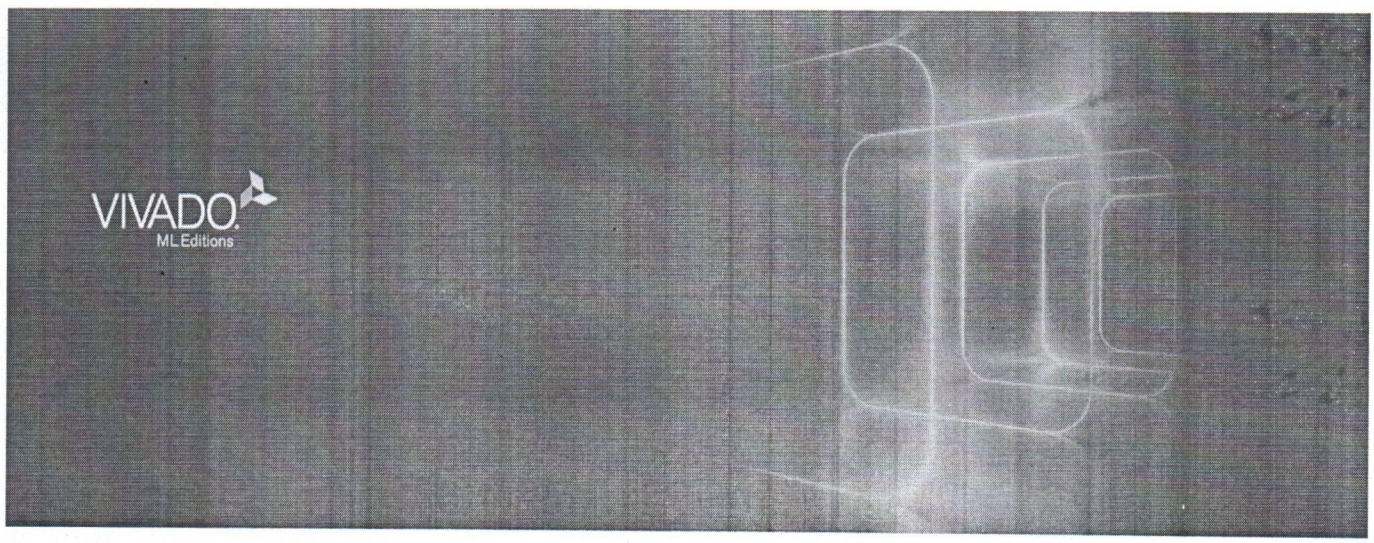
➢ **Expansion Connectors**

- 2xPmod ports
  16 Total FPGA I/O (8 pins on Pmod A are shared with Raspberry Pi connector)
- Arduino Shield compatible connector
  24 Total FPGA I/O
  6 Single-ended 0-3.3V Analog inputs to XADC
- Raspberry Pi connector
  28 Total FPGA I/O (8 pins are shared with Pmod A)

Vivado ML Enterprise



What's New in 2022.2 Key Highlights

- Introducing Power Design Manager for Versal® ACAP & Kria™ SOM
- Intelligent Design Run now supported for Versal devices shows average 5% QoR improvement over explore strategy *
- 1.4X compile time speed-up for UltraScale+™ architecture designs with Incremental Compile Flow **
- Abstract Shell for DFX now supported for Versal devices and in project mode
- DFX support enabled for Versal Premium SSI devices

Vivado ML What's New by Category

Expand the sections below to learn more about the new features and enhancements in Vivado® ML 2022.2.

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Device support

- Devices enabled in the Enterprise Edition of Vivado ML
    - Versal® Premium Series: XCVP1702, XCVP1802, XCVP1102
- Devices enabled in Standard and Enterprise Editions
    - Kria™ SOM: XCK24
- Devices that are production-ready
    - Versal Premium Series: XCVP1202
    - Versal Prime Series: XCVM1502
    - Versal AI Core Series: XCVC1702, XCVC1502

Install and licensing

- 25% reduction in peak disk footprint installation

IP enhancements

Infrastructure and Embedded

- Soft Endpoint Protection Unit (EPU) IP for protecting AXI agents residing in the PL

Storage

- Embedded RDMA enabled NIC (ERNIC) now supports up to 2k Queue Pairs (QP)

Gigabit Transceiver (GT) Wizard

- Versal GTMs now support rate switching between half and full density
- 16 configurations for Versal GTY/GTYP (limited to internal BRAM capacity)

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Wired

- 100G Multi-rate Ethernet MAC Subsystems (MRMAC)
  - Enabled 100G Ethernet 106G serial lane support
- 600G Multi-rate Ethernet MAC Subsystem (DCMAC)
  - Enabled 100GE, 200GE, 400GE 106G serial per lane support
- Aurora 64B/66B
  - Added support for 16 lanes of GTYP or Gigabit Transceiver Module (GTM) on Versal Premium

Wireless

- Zynq® RFSoC DFE IP Update: Channel Filter and DUC-DDC UL/DL sharing
- Zynq® RFSoC DFE DPD Update: PL resource reduction
- Zynq® RFSoC DFE O-RU TRD: Updated w/ Low PHY processing only

PCIe® Subsystems

- CPM5 x86 host drivers for Linux and DPDK in public release on GitHub
- Versal CPM5 PCIe BMD Simulation Design (from CED Store)
- Versal CPM Tandem PCIe Design (from CED Store)
- QDMA v5.0 improved performance/resource utilization

Multimedia

- Versal AI Edge enablement of soft IPs and Video Decoder Unit (VDU)
- Warp Processor IP in production
- Ultra HD 8K multimedia solution enablement for
  - HDMI2.1

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- Video Mixer IP

IP Integrator

- AXI streaming NoC MxN support in IP Integrator
- New address remap feature
- Vivado for default syntax checking
- Address path visualization
- XML to JSON format for XCI files

Simulation

- Support for System Verilog "Interface Class"
- Debug support for reference type System Verilog objects via tcl command and object window
- VHDL-2008 support

Hardware debug

- Support for PCIe Debugger on new Versal architectures
  - VP1502
  - VP1702
  - VP1802
- HBM2E Debugger support on Versal HBM devices

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- Integrated Bit Error Ratio Tester (IBERT) support on new Versal architectures
    - VP1502
    - VP1702
    - VP1802

Implementation

- QoR optimization for high fanout nets
- Placer replication for hard IP blocks
- Two new partitioning constraints for SSI designs
- LUT decomposition option to reduce congestion
- Incremental implementation enabled for monolithic Versal devices
- Support ECO flow for Versal devices

Timing closure

- New content added to QoR assessment report
- Average 5% QoR improvement for Versal designs when Intelligent Design Runs is enabled

DFX

- DFX support for SSI devices
- Abstract Shell support for Versal Premium and Versal HBM devices
- Abstract Shell support for project-based mode

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Vitis Software Platform 2022.2 Release Highlights:

Download Includes Vitis Core Development Kit

New Vitis™ Library Functions for Versal™ AI Engine (AIE) Arrays

- DSP library functions – enhanced features
- Solver library functions
- Vision library functions
- Ultrasound library functions

Design Flow Enhancements for Versal AI Core and AI Edge Series

- Control relative placement of kernels in the AI Engine array – higher performance and better utilization
- AIE x86 simulator enhancements - improved modeling of deadlock conditions in x86 simulator
- AIE API enhancements - Radix 3/5 FFT and Matrix 'x' Vector APIs added
- Enhanced profiling and debugging capabilities for Versal designs – deadlock detection, larger trace data collection, RTL/Python testbench support
- New simulation options for heterogenous designs in Vitis

Vitis What's New by Category

- Vitis Accelerated Libraries
- DSP library functions

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- Super sample rate (SSR) FIR filter implementation on AI Engine now supports coefficient reload feature and dynamic point size
- Added FFT windowing element to the FFT function that targets the AI Engine array

Solver library functions

- Quadrature rotation (QR) decomposition
- Cholesky decomposition
- Vision library functions
- Four new video functions targeting the AI Engine array
- Ultrasound library functions
- Various functions to help build medical ultrasound design
- Vitis AI Engine Compiler Features
- Ability to add constraints to control relative placement of kernels in the AI Engine array - this allows users to get higher performance and better utilization
- Improved modeling of AIE deadlock conditions in x86 simulator
- New AIE API added - Radix 3/5 FFT and Matrix 'x' Vector APIs added
- Vitis Profiling and Debugging Tools
- Generation of AI Engine profiling reports in HW Emulation
- Deadlock detection using XSDB (AMD System Debugger) for both AI Engine and PL-based designs

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- Xilinx Runtime (XRT) controlled continuous offloading of AI Engine event trace over PLIO
- Vitis New Simulation Options
- Supports PS application on x86 host machine for SW emulation
- Allows SystemC functional models for HW emulation instead of RTL
- Allows users to simulate the AI Engine kernel with a simple RTL test bench or Python script-based traffic generator
- AI Engine status can be analyzed during HW emulation with the Vitis™ analyzer

Vitis environment 2022.2 new simulation options: Processor system x86 simulation and AI Engine x86 simulation: Programmable logic simulation can be performed using the x86 simulator.

Vitis Model Composer

Features for Versal AI Engine Design

- Ability to add graph constraints to AI Engine DSP library blocks designs – better utilization and performance
- New capability for cycle approximate simulation for AI Engine designs
- AI Engine Graph Import block automatically detects Run Time Parameter (RTP) ports
- Enhancements and additions to the DSP Library blocks

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General Features

- Hardware validation flow supported for heterogenous system designs that use PL and AIE array
- Vitis Model Composer Hub block updated to support heterogenous design
- Automatic detection of valid AI Engine, HDL, and HLS subsystems
- Hardware validation flow enhanced for HDL only designs and HDL → AI Engine → HDL designs for Versal platforms

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