पं० रविशंकर शुक्ल विश्वविद्यालय, रायपुर (छ०ग०)

क्र0 139/विकास/2025 रायपुर, दिनांक 04/03/2025

।। दावा आपत्ति सूचना।।

सर्वसधारण को सूचित किया जाता है कि विश्वविद्यालय के उपयोग हेतु निम्नलिखित सॉफ्टवेयर सांपत्तिक प्रवृत्ति (Properietry Article) की श्रेणी के अंतर्गत क्रय किया जा रहा है :–

1. MATLAB Campus wide License (CWL) Software
2. Cadence VLSI University Research Bundle
3. VLSI Lab Tool Under CoreEL University Program
4. Silvaco Victory 3D Bundle Research Bundle

सांपत्तिक क्रय की श्रेणी के अंतर्गत क्रय के संबंध में किसी निर्माता कंपनी को यदि कोई आपत्ति हो तो दिनांक 04/04/2025 तक मयसुसंगत दस्तावेज विकास विभाग, पं.रविशंकर शुक्ल विश्वविद्यालय, रायपुर (छ.ग.) में प्रस्तुत करें। दिनांक 04/04/2025 के पश्चात प्राप्त दावा आपत्ति पर कोई विचार नहीं किया जायेगा।

4/3/25

कुलसचिव

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Date : January 6th 2025

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For Cadence Design Systems Ireland Limited

Authorized Signatory

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Claire Hinds
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Cadence Design Systems (Ireland) Limited
Date: _____

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LAB READINESS CONFIRMATION

COLLEGE NAME					
HOD		CONTACT		EMAIL	
LAB INCHARGE		CONTACT		EMAIL	
PLACE		DATE			

Suggested System Requirements and Lab Set-up

Operating System	Hardware Requirements				Operating System Requirements
	Hard Disk Space		Size of the RAM		
	Minimum (GB)	Recommended	Minimum (GB)	Recommended (GB)	
RHEL	Server: 500	Server: 1TB	Server: 16	Server: 32	*RHEL 7. 9 (64Bit) or RHEL 8.7 (64Bit)*
	Clients: 500	Clients: 1TB	Clients: 16	Clients: 32	

Note: Default Linux installation packages do not carry dependent files for running Cadence EDA Tools. Linux should be installed with full optional packages selected by choosing "Server With GUI" option at the time of installation. **A higher configuration system is recommended for the latest tools of Cadence. The system requirements vary with the design complexity. A lower or compatible version will be installed if the systems are of lower configuration. Kindly discuss with our executive if the system is of lower configuration.**

Along with these, below mentioned are some other requirements that are required for the set-up.

Sl. No	Description for Lab Readiness	
1	**Firewall must be disabled on all the client machines and the server. Has it been done?**	Yes ○ No ○
2	Server as well as the client machines should be assigned a static IP address and a hostname connected in LAN. **Has it been done?**	Yes ○ No ○
3	All the client machines should be able to ping the server with the IP address of the server as well as the hostname of the server with 0% packet loss. **(Please use ping command.) Has it been done?**	Yes ○ No ○
4	The client machines should also ping themselves with their respective hostname and the IP address. **Has it been done?**	Yes ○ No ○
5	Client machines' date and time should be in proper sync with the server. **Has it been done?**	Yes ○ No ○
6	A separate login can be created for the root and the user in the client machines. **Has it been done?**	Yes ○ No ○
7	Ftp and telnet should be enabled. **Has it been done?**	Yes ○ No ○
8	Server / Clients should have a DVD reader. **Has it been done?**	Yes ○ No ○
9	Host ID or Mac Address of the server should belong to "eth0" Ethernet port. **Has it been done?**	Yes ○ No ○
10	**Does the Server and Client machines are installed with Redhat Subscription?**	Yes ○ No ○
11	If Redhat Subscription is not available, install all the linux packages using the "Customize Now" option. ***Refer to the above youtube links for linux installation***	Yes ○ No ○
12	Linux Installation media and Lab Incharge / IT Admin should be available at the time of installation	Yes ○ No ○

Head of the Department
End User

(Signature and Seal)

Lab Instructor /

(Signature)

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Research Bundle Specification

- Conformal® GXL
- Conformal® Constraint Design L
- Conformal® Constraint Design XL
- CCD Multi-Constraint Check Option
- Conformal® Low Power
- Conformal® Low Power GXL
- Conformal® ECO Designer GXL
- Multi-Physics Universal HPC Token
- EMX® IC Solver
- Genus™ Low Power Option
- Genus™ Physical Option
- Genus™ CPU Accelerator Option
- Genus™ Synthesis Solution
- Cadence® Framework Integration Runtime Option
- Virtuoso® Simulation Environment
- Virtuoso® Schematic Editor HSPICE Interface
- Dracula® Graphical User Interface
- Cadence® SKILL Development Environment
- Virtuoso® EDIF 200 Reader
- Virtuoso® EDIF 200 Writer
- Cadence® Design Framework Integrator's Toolkit
- Virtuoso® Schematic VHDL Interface
- Virtuoso® Schematic Editor Verilog Interface
- Virtuoso® Analog oasis Run-Time Option
- Cadence® OASIS for RFDE
- Virtuoso® Analog HSPICE Interface Option
- Virtuoso® AMS Designer Environment
- Dracula® Physical Verification and Extractor Suite
- Diva® Physical Verification and Extractor Suite
- Virtuoso® Schematic Editor XL
- Virtuoso® ADE Explorer
- Virtuoso® Visualization & Analysis XL
- Virtuoso® ADE Assembler
- Virtuoso® Variation Option
- Virtuoso® ADE Verifier
- Virtuoso® DFM Option
- Virtuoso® Layout Suite GXL
- Virtuoso® Implementation Aware Design Option
- Virtuoso® System Design Platform
- Virtuoso® Layout Suite EAD
- Voltus™-Fi Custom Power Integrity Solution XL
- Voltus™-Fi Custom Power Integrity Solution - AA Advanced Analysis
- Virtuoso® Advanced Node Framework
- Virtuoso® MultiTech Framework
- Virtuoso® Advanced Node Option for Layout

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Virtuoso® Advanced Node Option for Layout Standard
Virtuoso® Photonics Option
Virtuoso® RF Platform
Virtuoso® Layout Suite EXL
Verifault XL Simulator
Verifault XL Slave Node License
Indago™ Debug Analyzer App
Indago™ Embedded Software Debug App
Virtuoso® Digital Implementation
Innovus™ 7nm Option
Innovus™ 20/16/14nm Option
Innovus™ Mixed Signal Option
Innovus™ High Frequency Route Option
Innovus™ Hierarchical Design Option
Innovus™ GigaPlace XL Option
Innovus™ Power Integrity Option
Innovus™ CPU Accelerator Option
Innovus™ Implementation System
JasperGold® RTL Designer Apps Option (to JGFVBASE)
JasperGold® Formal Apps Option (to JGFVBASE)
JasperGold® Advanced Platform Option to JGFVBASE
JasperGold® Formal Verification Platform
JasperGold® Coverage Unreachability APP
JasperGold® Verification Apps Option (Option to LGFVBASE)
Joules™ RTL Power Solution
Liberate™ Server
Liberate™ Client
Liberate™ LV Server
Liberate™ LV Client
Modus DFT Option
Modus Hierarchical Option
Modus ATPG
Innovus™ DFM Option
Litho Electrical Analyzer
Litho Physical Analyzer
Distributed Process for 8 CPUs
Cadence® Litho Hotspot Fixing Option
Generator to generate Assura® compatible verification decks
Generator to generate Diva® compatible verification decks
Error Cell Generator
Graphical Technology Editor
Pcell Generator

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Cadence® QuickView Layout and Mask Data Viewer
Cadence® QuickView Layout Data Viewer
Cadence® QuickView Sign-off Data Analysis Environment
Cadence® Physical Verification System Design Rule Checker XL
Cadence® Physical Verification System Layout vs Schematic Checker XL
Cadence® Physical Verification System Programmable Electrical Checker
Cadence® Physical Verification System Programmable Electrical Checker XL
Cadence® Physical Verification System Results Manager
Cadence® Physical Verification System Design Analysis Option
Cadence® Physical Verification System Design Review
Cadence® Physical Verification System Constraint Validator
Cadence® Physical Verification System Constraint Validator XL
Cadence® Physical Verification System Advanced Analysis Option
Cadence® Physical Verification System Advanced Device Option
Cadence® Physical Verification System Pattern Matching Option
Cadence® Physical Verification System Mask Rule Check Option
Cadence® Physical Verification System Results Viewer
Virtuoso® Integrated PVS Option for Layout Suite
Cadence® Quantus™ Extraction XL
Cadence® Quantus™ Advanced Analysis GXL Option
Cadence® Quantus™ Advanced Modeling GXL Option
Cadence® Quantus™ Display Technology Option
Cadence® Qunatus™ Advanced Modeling20 GXL Option
Cadence® Quantus™ Advanced Node Modeling Option
Quantus™ 32/28nm to 10nm Option
Aurora
Advanced SI
Advanced PI
Advanced IBIS Modeling
Celsius™ Thermal Solver
Celsius™ CFD Extension
Clarity™ 3D Solver
Clarity™ PCB Extraction Suite
Clarity™ IC Package Extraction Suite
Allegro® PCB Symphony Team Design Option
Allegro® Venture PCB Designer
Cadence® 3D Design Viewer
Allegro® AMS Simulator
Allegro® PCB Librarian
Allegro® Venture System Design Authoring
OrbitIO™
SiP Layout Option

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- APD Silicon Layout Option
- Allegro® Package Designer Plus
- Spectre® Characterization Simulator Option
- Spectre® RelXpert Reliability Simulator
- Interactive mode for Spectre® using Python/TCL
- Spectre® AMS Designer
- Spectre® MMSIM with Spectre X Simulator
- Spectre® Power Option
- Spectre® CPU Accelerator Option
- Spectre® Extensive Partitioned Simulator
- Tempus™ Timing Signoff Solution L
- Tempus™ Timing Signoff Solution XL
- Tempus™ Timing Signoff Solution ECO
- Tempus™ Timing Signoff Solution MP
- Tempus™ Power Integrity Option
- Voltus™ IC Power Integrity Solution XL (VTS-XL)
- Voltus™ IC Power Integrity Solution GXL Option (VTS-AA)
- Voltus™ IC Power Integrity Solution ESD
- Voltus™ IC Power Integrity Solution MP (VTS-MP)
- Stratus™ HLS XL
- vManager™ Safety
- vManager™ Linux Client (Quantity 5)
- vManager™ Project Server
- Enterprise Simulator XL Interface for MTI
- Enterprise Simulator XL Interface for VCS
- Xcelium™ Single Core
- Xcelium™ Digital Mixed Signal Option
- Xcelium™ Safety Simulation

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AGENDA FOR POST INSTALLATION TRAINING

Day 1

FULL CUSTOM DESIGN FLOW

- Introduction to Full Custom IC Design Flow
- Cadence Solutions for Custom IC Design
- Schematic Capture using Virtuoso Schematic Editor
- Symbol Creation
- Testbench Creation using Virtuoso Schematic Editor
- Functional Simulation using Spectre
- Layout Design using Virtuoso Layout Editor
- Physical Verification which includes DRC & LVS
- Parasitic Extraction using Quantus
- Post Layout Simulation
- Generation of GDSII

Note:

- The entire Full Custom IC Design Flow will be demonstrated by considering CMOS Inverter as an example.
- 1-day Training for new customers.
- The same case study will be demonstrated for renewal orders as a half-day session.

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Day 2

SEMI-CUSTOM DESIGN FLOW

- Introduction to Semi-Custom IC Design Flow
- Cadence Solutions for Semi-Custom IC Design
- Functional Verification using Incisive
- RTL Synthesis using Genus Synthesis Solution
- DFT (Design for Testability) using Modus
- LEC (Logical Equivalence Check) using Conformal
- Physical Implementation using Innovus that includes
  - ✓ Floor Planning
  - ✓ Power Planning
  - ✓ Placement
  - ✓ CTS
  - ✓ Routing
- Timing Analysis using Tempus
- Power Analysis using Voltus
- Parasitic Extraction
- Generation of GDSII

Note:

- The entire Semi-Custom IC Design Flow will be demonstrated by considering 8-bit Counter as an example.
- 1-day Training for new customers.
- The same case study will be demonstrated for renewal orders as a half-day session.

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Day 3

ALLEGRO DESIGN FLOW

1.0 – Electronic Product Design Cycle

2.0 – Design Entry (Schematic): Design Example – Hands On

2.1 – Working with projects and its configuration

2.2 – Parts Manager

- ☐ Add parts in parts manager
- ☐ Search the parts – Global/Local Search
- ☐ Parts placements
- ☐ Object alignment and distribute

2.3 – Wiring your circuits: Auto/Manual/Virtual Wiring

2.4 – Annotate your circuit

2.5 – Property Editor: Parts/Pins/Nets

3.0 – Generate the BOM (Bill of Material)

4.0 – Introduction to PCB and Layout Design Process: - Hands On

4.1 – Prepare your circuit for layout design

4.2 – Package Mapping and net list generation for Layout design

4.3 – Design stackup and Layout configuration (Floor planning)

4.4 – Create board outline and Package Keep out area

4.5 – Component Placement and Alignment

- ☐ Placement techniques : Understand the importance of parts placement in Layout
- ☐ Auto Placement/Manual
- ☐ Component Alignment
- ☐ Define spacing constraint b/w component to component and component to obstacle – Constraint Manager

4. **6 – Route the Layout**

- ☐ Trace width calculation
- ☐ Define constraint for routing : constraint Manager
- ☐ Interactive routing : Push, Shove and Hug
- ☐ Routing editing
- ☐ Waive DRC and Identify the error
- ☐ Editing Tools and Techniques

5.0 – Generate Fabrication Files/Data for Layout

5.1 – Generate Auto Silk Screen

5.2 – Create NC Drill (Numerical Control)

5.3 – Generate Artwork files/ Gerber Files